TP1345

ENGINEERING FINAL REPORT

OCTOBER 1965

DATA LINK EQUIPMENT
FOR
SATURN
GROUND COMPUTER SYSTEMS
NAS 8-11582

PREPARED FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

WEST COAST DIVISION
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8500 BALBOA BLVD.,
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ABSTRACT

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This is the final technical report on the Data Link system and equipment designed and developed for NASA under contract NAS 8-11582. This report is submitted in accordance with the requirements of Contract NAS 8-11582.

This report is primarily technical in nature. The objective being to present the technical results of the program and design philosophies adopted. The intent is to disclose why the equipment and systems resulting from the execution of the contract have certain operational characteristics. The functional operations of the system and equipment are explained in detail in the Saturn Data Link Terminal Instruction Manual, TP1245, which was published under provision of Contract NAS 8-11582.

A review of the major program milestones and accomplishments is presented in Section 1 of this report. Section 2 contains a description of the system requirements and specifications including a general review of contract modifications. Section 3 outlines the program plan and describes the tasks assigned to the various RCA departments included in the program. Section 4 contains a functional description of the system assemblies including the Power System and Cable Simulator. A detailed description of the design and fabrication of the Data Link equipment is presented in Section 5 while Section 6 contains a description of the system reliability testing. Section 7 contains a description of the programs generated for use with the Data Link system. In Section 8, RCA presents a recommendation for the initiation of a field evaluation program to establish the performance characteristics of the Data Link system under actual operating conditions. As an aid to this program, the performance characteristics of the system, as observed under laboratory operating conditions, have been included in the Appendix to this report.

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SECTION 1

INTRODUCTION

PROGRAM MILESTONES

The contract NAS 8-11582 was awarded to RCA, Van Nuys on 3 April 1964, covering the design, fabrication, checkout, delivery and installation of six Data Link Terminals.

1.1 IMPLEMENTATION PLAN

A detailed Implementation Plan for the design, operation and checkout of the Data Link Terminal was developed and the design work commenced.

1.1.1 Engineering Schedule

In May 1964 milestones for the release of material and drawings to manufacturing were established and a detailed engineering schedule was prepared. The Data Link modem was defined in sufficient detail to negotiate a contract with RCA CSD Tucson. A work order was released to RCA CSD with an effective start date of 22 May 1964.

1.1.2 Plan Presentation

A presentation was given to NASA at Huntsville in June 1964 to explain the detailed implementation plan. The presentation was followed up with a deviation request for customer approval.

1.2 PROGRAM PROGRESS

1.2.1 Mechanical Parts Release

In June 1964, mechanical purchased parts for the cabinet, control logic assembly, and Data Modem assembly were released to manufacturing. Mechanical drafting and fabrication of the control panel and the power control sequencer was started.

1.2.2 Design Review

In June 1964, the final design review for the control logic and the electrical concept review for the power control sequencer were completed. A revision to the modem specification was made to assure compatibility with the equipment and to classify modem requirements.

The block diagram of the modem was developed and approved by a concept review. Work was started on the design of special module boards unique to the data modem.

1.2.3 Release to Manufacturing

In July 1964, the Data Link System Cable and Installation Specification NSI 519 was submitted to NASA. Electrical and mechanical design was completed on the control logic assembly and control panel and wire lists were released to Manufacturing. Electrical design on the power sequencer assembly was completed. Mechanical design of the terminal assembly was about 80 per cent completed and awaiting details of the customer interface requirements. Drafting and fabrication to support the design effort was progressing satisfactorily. RCA CSD Tucson completed all concept design reviews and work on new module boards was progressing toward final release to RCA Camden for fabrication. A Breadboard Modem was wired to be used for design evaluation.

1.2.4 Subassembly Release

During the month of August 1964 all Data Link subassemblies were released for purchase or fabrication. A special test equipment nest and rack was fabricated. This equipment has permitted a partial checkout of the control logic assembly without a Data Modem at RCA, Van Nuys. NASA grounding, RFI, and seven-mile cable termination requirements had not been clarified. This, together with the fact NASA considered a change in the connector to be used for the seven-mile cable interface, did not enable the release of connector housings and cable assembly drawings with the cabinet top assembly drawing at this time. The Data Link top assembly drawings were released 14 September 1964.

1.2.5 Design Evaluation

In September 1964, the design evaluation of the Control Logic, Maintenance and Control assemblies for Terminal No. 1, System No. 1, was started by engineering. The major design review of RCA CSD Data Modem circuits began on 28 September 1964.

During the same month a proposal effort was conducted in accordance with Mod. No. 5 to the contract to convert the third system to Saturn V compliance.

Parts procurement and late changes resulting from worse case analysis of the special modem printed circuit boards caused delivery of these boards to slip CSD's schedule.

1.2.6 Control Logic Tests

Tests of the Control Logic and Control Panel with the 110A IODC and the computer were started during October 1964. Debug programs were generated and run with this test set-up. The first production power sequencer was tested independent of the rest of the system. Wiring of the production modems was started. CSD module board documentation was released and the initial lot of modules built at the RCA Camden plant.

1. 2. 7 Engineering Evaluation

The Engineering evaluation testing of Data Link System No. 1 took place in November 1964 and continued through December 1964. This evaluation involved both terminals of the first system, two prototype Data Link IODC's, and an SIB Computer. Breadboard Modems were used for this testing. Noise injection tests uncovered some problems in the demodulation logic and these problems were corrected. The first cable simulator set built at CSD was delivered to RCA Van Nuys in early November 1964.

The first production lot of special Data Modem module boards was received in CSD-Tucson in December 1964, and used to check out the first production Data Modem. The system was tested on 30 December 1964, to an acceptance test procedure, and witnessed by RCA Van Nuys engineering. After the joint CSD/RCA Van Nuys acceptance tests on System No. 1 were successfully completed, CSD was requested to hold shipment of the System No. 1 Modems, while a determination was made to see if NASA representatives wanted to witness the Modem testing. A meeting was held at RCA Van Nuys on 9 January 1965 in which NASA technical representatives and two Bellcomm NASA consultants participated. The meeting covered the RCA Data Link testing philosophy from the component to the system level. Plans for a proposed field cable evaluation were also discussed at this meeting.

1. 2. 8 System No. 1 Modem Acceptance Tests

The System No. 1 Modem acceptance tests were rerun on 13-15 January 1965 at CSD Tucson with NASA representatives in attendance. In addition to the tests outlined in the Acceptance Test Procedure, additional tests were run for the NASA representatives to provide an additional confidence level. The NASA representatives were satisfied with the Modem performance based on the results of the acceptance tests and the additional tests conducted.

The System No. 1 Modems were delivered to RCA Van Nuys on 18 January 1965. In addition, two copies of each schematic, logic diagram, wire list and copper path list were delivered to Van Nuys.

Engineering tests on Data Link System No. 1 continued during January 1965 with the two Breadboard Modems, which were installed in cabinets. Final System Testing with the end item Modems was underway by the end of January 1965. Five copies of the Data Link Preliminary Instruction Manuals were submitted to NASA on 8 January 1965.

1.2.9 System Demonstration

The first Data Link System was successfully demonstrated to NASA Technical and Quality personnel, as well as Air Force Quality, on 13 February 1965. A preliminary issue of NSI-532 served as a demonstration procedure. The first system was retained at RCA Van Nuys for the 1000 hour reliability test.

1.2.10 Data Link System No. 2

Data Link System No. 2, an SIB configuration, was in final wiring at the end of January 1965. The Data Modems were received at RCA Van Nuys and installed in the second system terminal during February 1965.

1.2.11 Data Link System No. 3

Data Link System No. 3 was converted to the SV configuration. All SV releases were made during February 1965, including the specially designed Data Modem parts.

1.2.12 System Allocations

Data Link System No. 2, allocated to the SIB Breadboard facility, was demonstrated to NASA in Van Nuys on 12 March 1965. The cabinets were shipped on 16 March 1965 and were installed and checked out at the SIB Breadboard facility. Acceptance by NASA was completed on 27 March 1965.

Data Link System No. 3, an SV configuration, was allocated to Complex 34-LCC at Kennedy Space Center. The cabinets were assembled and wired during March and

April 1965 at which time the two Data Modems for this system were in production at the CSD Tucson facility.

In March 1965 all technical inputs were submitted to Publications and work proceeded on final manual clean-up.

The 1000 hour test on Data Link System No. 1 was completed on 27 April 1965. This system, allocated for the MSFC Astrionics Laboratory, was scheduled to operate with SIB Computer No. 1, produced under Contract NAS 8-5423. Since this computer underwent Acoustic and Vibration Testing at Wyle Laborabories at Huntsville, Alabama, the Data Link System No. 1 was held at Van Nuys, awaiting NASA's direction to ship.

Assembly and wiring of Data Link System No. 3 cabinets was completed in May 1965. The two SV Data Modems were also received in May 1965. The System completed final testing in early June 1965 and was demonstrated to the Air Force. The system was shipped from Van Nuys on 12 June 1965 and installed with SV Computer System No. 2 at Cape Kennedy and accepted by NASA on 24 June 1965.

Reliability calculations for the Modem were completed and the Detailed Reliability Estimate for the Saturn V Data Link Systems was published in June 1965.

The 1000 hour Reliability Report was published as part of the Data Link Systems Reliability Progress Report in June 1965.

Data Link System No. 1 was shipped from Van Nuys in June 1965, installed in July and together with the computer was accepted by NASA at the Astrionics Laboratory on 20 September 1965.

The rough draft of the Data Link Design Specification was completed in June 1965. The final copy was submitted to NASA during July.

Delivery of Cable Simulators was accomplished in October 1965.

SECTION 2

SYSTEM REQUIREMENTS AND SPECIFICATIONS

This section contains a general review of the contract, key contract specifications, and contract modifications.

2.1 GENERAL REVIEW OF CONTRACT

2.1.1 System Description

The Saturn Data Link System consists of two identical cabinets which provide two-way communication over a a video cable up to seven miles long.

Figure 2-1 illustrates an application in which the Data Link provides realtime communications between two 110A computers.

2.1.2 Purpose of System

The Saturn Data Link System operates as an integral part of the dual RCA 110A ground computer system. The Data Link permits an exchange of command and data messages between two RCA 110A computers via their Input/Output Data Channels (IODC). Both message types are transferred accurately and reliably with the aid of a two dimensional parity check which initiates a repeat request when errors are detected.

2.1.3 Statement of Work

Contract NAS8-11582 covers the design, fabrication, checkout, delivery and installation of six (6) Data Link Terminals with the specifications and characteristics delineated under subject contract and as modified through Modification 15.

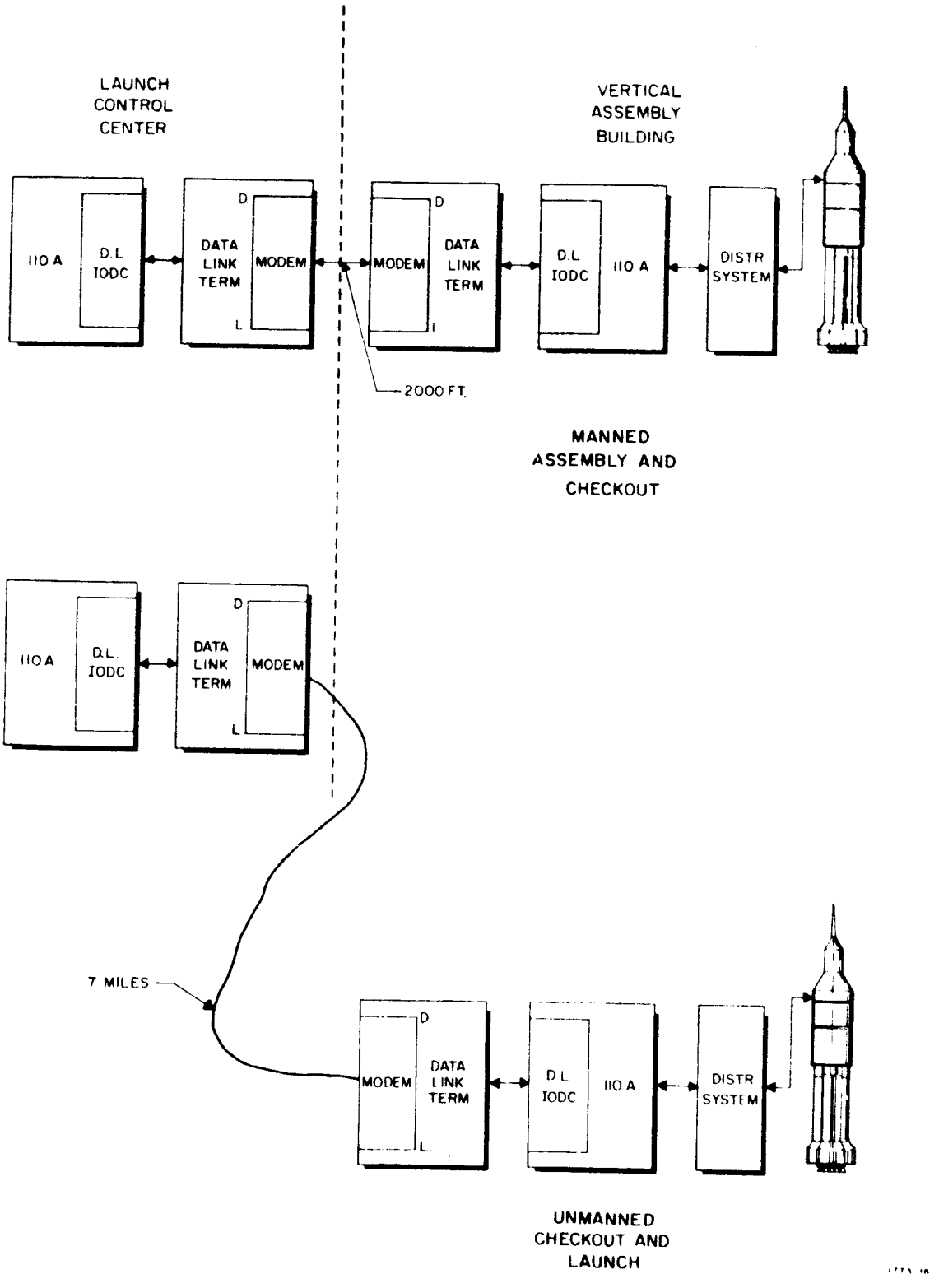

Figure 2-1. Saturn Data Link Applications

2.2 GENERAL REVIEW OF KEY CONTRACT SPECIFICATIONS

2.2.1 Packaging

Each Data Link terminal will be packaged in a separate RFI-proof cabinet of the RCA-110 design. Provisions of MIL-I-6181D will be applied but testing for conformance is not a requirement. Packaging techniques must take into consideration the possibility that data link equipment will be required to operate correctly in an acoustic environment of 130 db (0.0002 dyne/cm^2 ref) over a frequency range of 20 cps to 10 kc, while experiencing conductive vibration of a 1g level over the same frequency range. Equipment must operate reliably and accurately in air ambient temperature of 60°F to 80°F.

2.2.2 Information Transfer

Information transfer between the computer IODC and the Data Link terminal will be serial. Information transmission between terminals will be at a minimum gross rate of 250 kilobits/sec with the remaining redundant bits added for necessary coding and error detection to provide a probability of an undetected error 2.8×10^{-14} words/word, based on Gaussian or White noise environment resulting in 10^{-4} single bit error rate. Command information will be full duplex and data information will be one-half duplexed between data link terminals. Transmission errors due to Gaussian and impulse noise must be a consideration in the coding and detection circuitry.

2.2.3 Transmission Capability and Operation

RCA was directed to insure that the Data Link be capable of accurate and reliable operation when separation between computer IODC and a terminal is upwards to 100 electrical feet and the separation between terminals is 2000 feet to seven (7) miles.

2.2.4 NPC 250-1 Compliance

RCA was directed to establish and maintain an effective reliability and test program to satisfy the requirements of the July 1963 edition of the NASA Reliability Publication NPC 250-1. The design reliability goal was 0.99 for seven (7) hours of equipment operating time.

All parts and circuits of the Data Link Systems that were not previously designed for use within the RCA 110A Computer System were to be presented for MSFC approval prior to purchase and fabrication.

2.3 GENERAL REVIEW OF CONTRACT MODIFICATIONS

2.3.1 Saturn V Requirements on Third Data Link System

RCA was directed on 12 August 1964 to fabricate the third data link system under Contract NAS 8-11582, utilizing those parts approved by MSFC for the Saturn V (Contract NAS 8-13007), RCA 110A Computer system. Any change in the Saturn V approved parts due to new design was required to be submitted to MSFC for review as defined within NPC 250-1.

2.3.2 Approved Deviation Request - Contract NAS 8-11582

The status deviation requests on Contract NAS 8-11582 is shown below. The deviations for this contract were either of a minor nature or were design improvements implemented early in the program and already incorporated in the operational systems.

001	---	Cancelled by RCA.
002	8-25-64	Improvement of system operation reliability, maintainability and timing efficiency.
003	8-7-64	Tubing must be used over solder connections where danger of shorting exists.
004	8-18-64	Change from 3-word to 2-word retransmission. Improves reliability.
005	10-19-65	Make isolation resistance measurements with voltohmyst.

006	10-8-64	Cable simulator simulates cable at one-half mile increments.
007	3-6-65	No special mounting of VO41 and preamplifier one-half ounce components
008	9-8-65	Approves use of water soluble flux on 56 Cable Simulator Boards.

2.3.3 Modifications to NAS8-11582

The following modifications have been issued on Contract NAS 8-11582 and apply to the Data Links in systems 2112000-503, -504, -509, and -510.

Mod. No. 1, 12 June 1964.	Increases funding.
Mod. No. 2, 24 June 1964.	Amends "Place of Performance" to include CSD, Tucson, Arizona.
Mod. No. 3, 18 August 1964	Imposed revised issue of MSFC-PROC-293A in lieu of MSFC-PROC-293.
Mod. No. 4, 8 Sept. 1964	Increases funding.
Mod. No. 5, 11 Sept. 1964	Authorizes fabrication of the third Data Link using parts approved for the Saturn V RCA-110A computer system.
Mod. No. 6, 10 Nov. 1964.	Grants waiver of MSFC-PROC-186 as called out in MSFC-PROC-293A.
Mod. No. 7, 22 Nov. 1964.	Changes requisition shown on Mod. No. 3.
Mod. No. 8, 22 Dec. 1964.	Provides specific destinations for each system.
Mod. No. 9, 23 Feb. 1965.	Increases funding.
Mod. No. 10,	Modifies Period of Performance: "to require that all work and services to be completed on or before 30 June 1965."
Mod. No. 11, 30 April 1965.	Increases funding and clarifies minor contract clauses.
Mod. No. 12, 2 June 1965.	Changes requisition number on a previous change order.
Mod. No. 13,	Modifies period of performance: "to require that all work and services be completed on or before 31 August 1965."
Mod. No. 14,	Modifies period of performance: "to require that all work and services be completed on or before 31 October 1965.
Mod. No. 15, 11 October 1965.	Not fully executed. Adds ECP 110A-49671-0079 for all Data Links except 2112000-503 and -504.

SECTION 3

PROGRAM PLAN

A list of RCA organizations that participated in the Data Link program and their respective contributions is presented below.

- RCA DEP-Camden Manufacturing.
  All printed circuit assemblies used in the Data Link equipment were fabricated, assembled, and tested by the Camden Printed Circuits Manufacturing activity which has been inspected and approved by NASA.

- RCA CSD-Tucson Engineering.
  This organization performed engineering activities associated with the Data Modem assembly and Cable Simulator assembly. Specific contributions were:

  a. Design and development of the Data Modem and Cable Simulator.

  b. Perform associated test and evaluation activities.

  c. Generate documentation to support manufacturing, testing, manual and report publications, and design review efforts.

  d. Perform liaison with component vendors and Camden Manufacturing concerning manufacture of new design modules.

- RCA CSD-Tucson Manufacturing.
  Data Modem assemblies delivered under this contract were fabricated, assembled and tested by this activity. Completed units were shipped to RCA Van Nuys for system integration.

- RCA Van Nuys Engineering.

  This organization performed engineering activities associated with the Data Link system, specifically:

  a. Provide technical management.

  b. Design and development of the Data Link terminal.

  c. Generate Saturn 110 Computer programs and programming techniques to test, evaluate, and utilize the Data Link system.

  d. Perform system test and evaluation activities.

  e. Generate documentation to support manufacturing, testing, manual and report publications, and design review efforts.

  f. Prepare and maintain cognizance over purchased part specifications.

  g. Perform purchased part qualification testing and control activities.

  h. Prepare detailed system reliability estimates and recommended changes that would improve system reliability.

  i. Perform technical liaison activities with NASA, CSD-Tucson, field installation groups, and internal manufacturing organizations.

- RCA Van Nuys Program Management.

  Van Nuys Program Management performed the following tasks associated with the Data Link program:

  a. Coordinate program with NASA.

  b. Authorize and direct engineering, materials and manufacturing operations.

  c. Fund tasks.

  d. Interface with contract administration, operations control, and general manager.

  e. Impose contract requirements.

- RCA Van Nuys Manufacturing.

  Van Nuys Manufacturing performed all activities associated with the fabrication, assembly and testing of Data Link terminals. Specific major items were:

  a. Fabricate, assemble, and test Data Link terminals.

  b. Perform RCA quality control functions.

  c. Prepare production unit test procedures.

  d. Maintain cognizance over material, component, and subsystem procurement required to fulfill production schedules.

In general, the program plan was to perform the various tasks required to fulfill the contract in parallel as much as possible. This approach was required because of the short time duration between contract award and equipment specified delivery dates.

Once the general system design was completed, the detailed design of the Data Link subsystems proceeded simultaneously. Component purchasing authorizations were released as soon as designs became relatively firm. Requisitions for power supplies were prepared and released during the first week of the detailed design effort, and preliminary printed circuit module board requirements were released within the first month. Mechanical components and chassis were fabricated from engineering sketches at the same time drafting groups were preparing detailed drawings. As soon as the drawings were released the fabricated parts were subjected to appropriate quality control inspection and released for assembly.

The first Data Link subassemblies completed by Manufacturing were utilized by Van Nuys Engineering for prototype testing and evaluation. Required equipment changes to the prototype subassemblies and following units were incorporated. The prototype units were tested, evaluated, and assembled into complete Data Link terminals in the Engineering Laboratory through the cooperation of Van Nuys Manufacturing and Engineering organizations. To aid in this accelerated effect, RCA CDS-Tucson delivered

to Van Nuys two Breadboard Data Modem assemblies for use in system evaluation until production assemblies were available.

The two Data Link prototype terminals were subjected to full quality control inspection and all equipment changes were incorporated. The two terminals were assigned serial numbers 030-0001 and 030-0002. These units were demonstrated to NASA, used in a 1000 hour reliability test, and then installed in computer facilities at MSFC, Huntsville, Alabama. These two terminals were the last of six to be delivered under contract NAS 8-11582.

SECTION 4

MAJOR DATA LINK COMPONENTS

4.1 DATA MODEM ASSEMBLY

4.1.1 Functional Description

The Data Modem assembly is designed to convert non-return-to-zero (NRZ) digital information from the Data Link Control Logic into modified diphase signals suitable for transmission over a balanced video cable up to seven miles in length. It demodulates received modified diphase signals, converts the information to NRZ digital form, and supplies this information to the Data Link Control Logic for processing. The Data Modem assembly also generates timing signals for the entire Data Link system.

The Data Modem assembly consists of four functional units:

- Modulator.
- Demodulator.
- Locked Timer.
- Master Timer.

4.1.2 Modulator

The Modulator accepts NRZ digital data along with digital timing information from the Data Link Control Logic and converts this information into modified diphase signals. These modified diphase signals are then transmitted over a balanced video cable which terminates in the Demodulator of the second Data Modem located at the receiving end of the video cable. Figure 4-1 illustrates modified diphase signals.

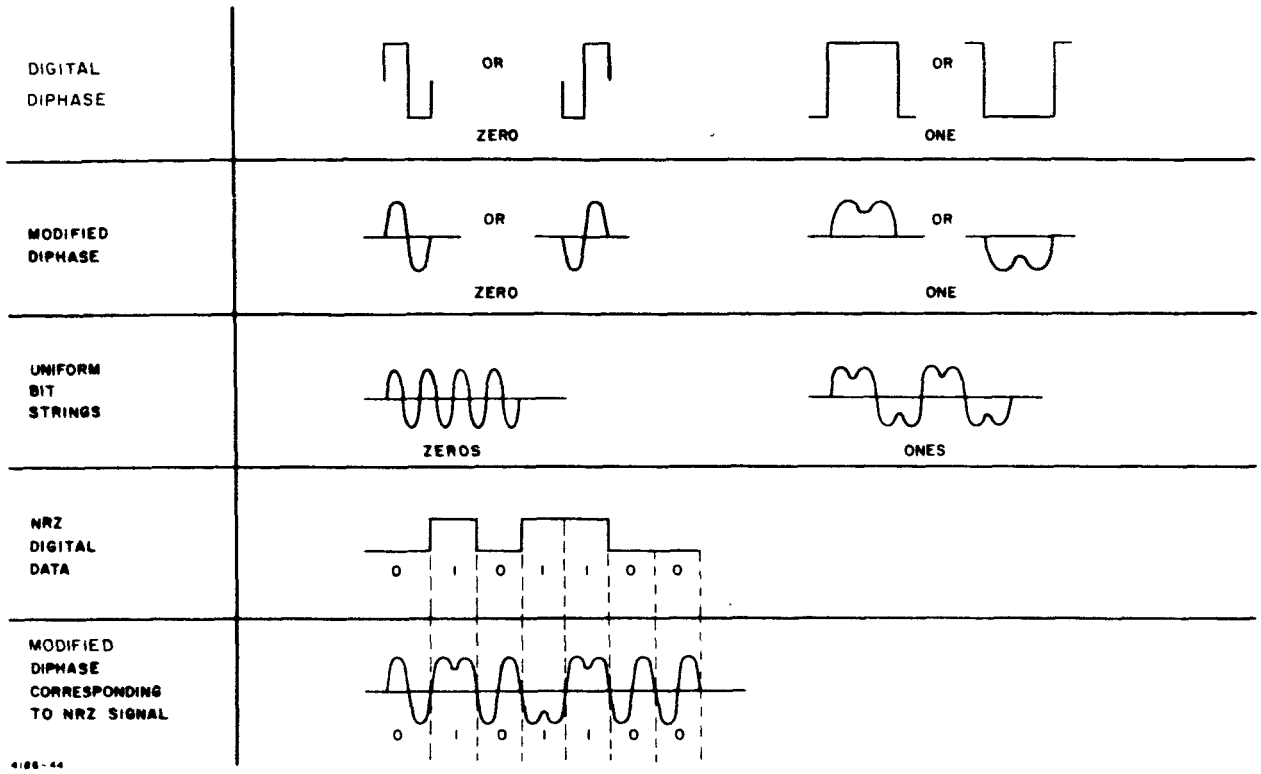

Figure 4-1. Diphase Signals

4.1.3 Demodulator

The Demodulator receives modified diphase signals from the video cable, extracts NRZ digital information from it, and supplies this information to the Data Link Control Logic.

4.1.4 Locked Timer

The Locked Timer generates clock signals at a 250 kilohertz rate. These signals are phase-locked to the received diphase signal. This clock is the timing source for the processing of all received information. It is also the timing source for transmitted information in the Data Link Terminal designated as "Slave" in the Data Link system.

4.1.5 Master Timer

The Master Timer is a free-running, 250 kilohertz, clock source. It is the timing source for transmitted information in the "Master" Data Link Terminal. Since the other system clock source, the Locked Timer, is phase-locked to received signals, the Master Timer is the master or primary timing source for the entire Data Link system.

4.2 CONTROL LOGIC

4.2.1 Functional Description

The primary function of the Data Link Control Logic (see Figure 4-2) is to reliably and accurately control the message transfer between two Saturn Ground Computers. This is accomplished by:

- Monitoring all received messages, for correct parity.
- Detecting and correcting errors which may be introduced by noise.
- Monitoring message origin and thereby determining message destination.
- Maintaining word sequence at all times.

4.2.2 Interfaces

The Data Link Control Logic interfaces with a Saturn 110 Ground Computer through an Input/Output Data Channel assembly within the computer, and with the Data Modem assembly. The IODC provides the capability of transferring information between the computer and the Data Link System simultaneously with normal computer processing.

4.2.3 Transmitter

The transmitter is a functional unit of the Data Link Control Logic and is so named because it accepts messages from the IODC and transmits them, via the Data Modem, to the remote terminal. The message which is transmitted by the Control Logic is

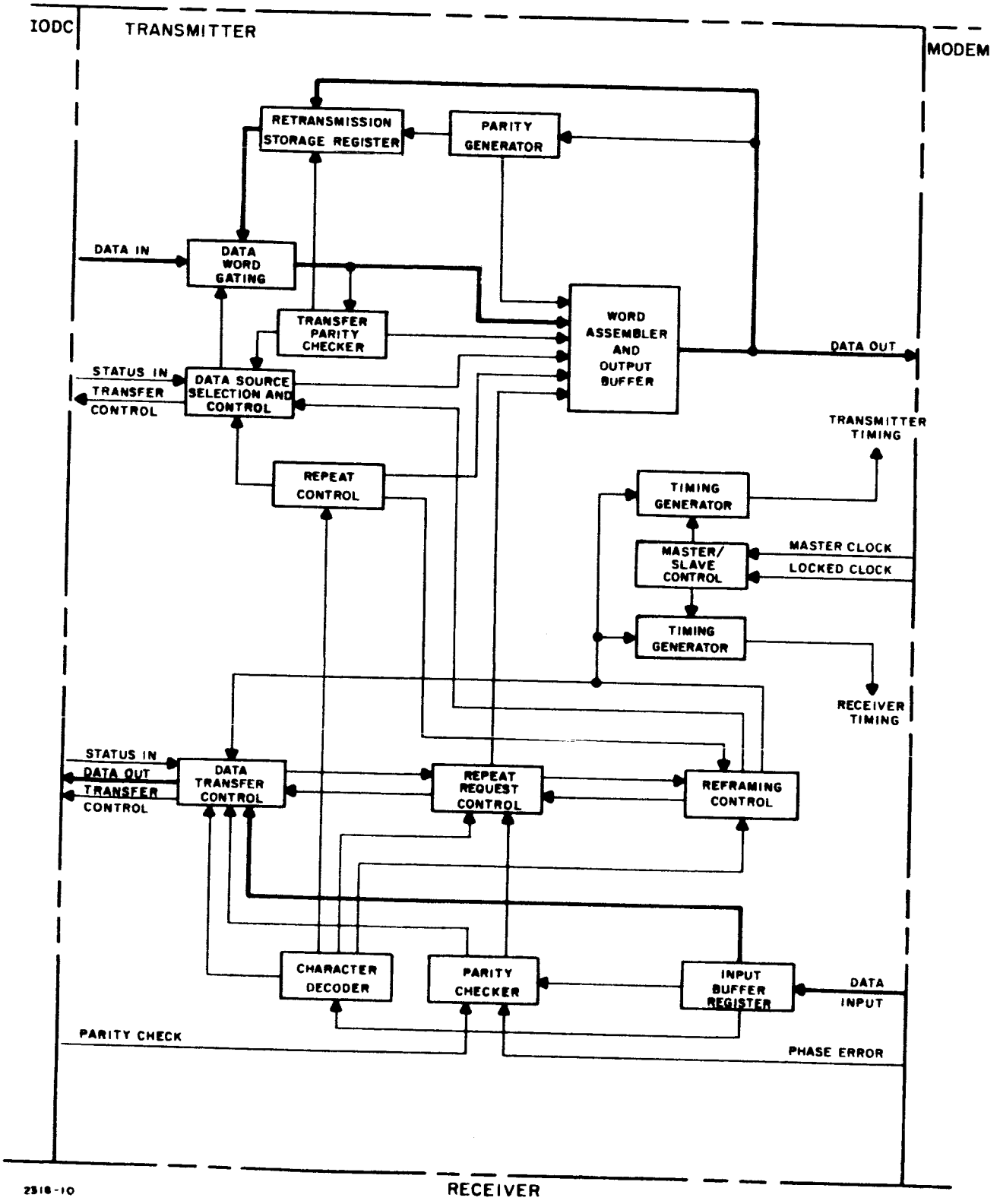

Figure 4-2. Data Link Block Diagram

unique in structure. It contains the 24 data bits, which comprise the standard Saturn computer word, and 21 additional bits which are inserted by the Control Logic transmitter for error detection and correction and for message origin and destination information.

4.2.3.1 Retransmission Storage Register

All words transmitted are also retained by the Control Logic in the Retransmission Storage Register. This shift register is of sufficient length to store the data portion and origin information of two consecutive words. If a word is found to be erroneous by the remote terminal, an automatic repeat request is generated by that terminal. The local control logic then retransmits the contents of the retransmission register with all the required error detection bits added.

Word sequence is always maintained in that the second word of any transmission will not be accepted by the remote terminal as long as the preceding word contains an error.

4.2.4 Receiver

The receiver section of the control logic receives digital information from the Data Modem and performs the following major functions:

- Checks incoming messages for errors thereby determining whether or not a request for retransmission shall be generated.
- Routes incoming messages to their correct destination.
- Determines whether or not a request for retransmission was generated by the remote terminal and notifies its transmitter to take appropriate action.
- Performs various data interrogation and processing functions for the purpose of verifying system synchronization.

4.3 MAINTENANCE AND CONTROL ASSEMBLY

4.3.1 Functional Description

The Maintenance and Control assembly is a panel with functionally grouped switches and indicators which permit manual and visual interface with the Data Link terminal. This assembly is illustrated in Figure 4-3.

4.3.2 Control Switches

Control switches are provided for the purposes of power control and for manual check-out of the Data Link in an off-line or test mode.

4.3.3 Test Switches

Test switches are provided to permit a manual test of all major Data Link functions without requiring computer intervention.

4.3.4 Alarm and Status

Indicators are provided to permit monitoring the data transfer between terminals; to indicate certain error conditions, and to show when the ambient temperature in the Data Link cabinet exceeds a predetermined value.

4.4 POWER SYSTEM

4.4.1 Functional Description

Each Data Link Terminal has a complete, self-contained, DC power system consisting of three power supplies and a Sequencer Power Control assembly.

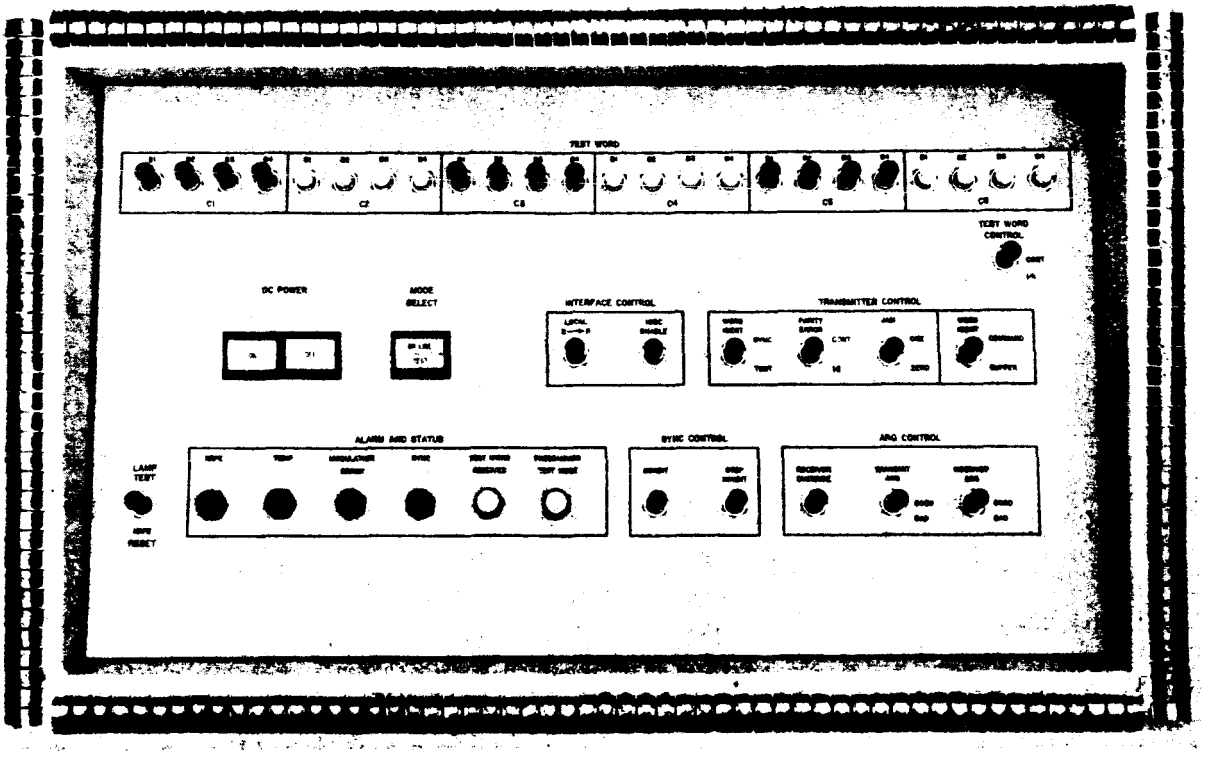

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Figure 4-3. Control Panel

4.4.2 Power Supplies

The three power supplies are identical, general purpose, units. They have adjustable voltage ranges and have operational properties compatible with all Data Link circuit requirements.

4.4.3 Sequencer, Power Control

The Sequencer, Power Control assembly controls the application of DC power to the Data Link circuit modules. During normal power ON and OFF cycles, the voltages are applied and removed in a sequential manner.

Various voltage sensing circuits are provided for the detection of power system malfunctions that could be destructive to the Control Logic and Data Modem circuits. If

such a malfunction is detected, the DC voltages are automatically removed from the circuit modules. Provisions are also made to permit maintenance and testing of the power system without requiring voltage application to the circuit modules.

4.5 CABINET ASSEMBLY

The Data Link cabinet is a Standard Saturn 110 Computer, double-rack, cabinet. Various mechanical brackets and fixtures are provided for mounting the sub-assemblies associated with the Data Link Terminal (refer to Figure 5-14). These sub-assemblies are:

- Data Modem.
- Maintenance and Control Assembly.
- Control Logic.
- Sequencer, Power Control Assembly.
- Power Supplies.
- Blowers.

The Data Link cabinet front door is a special design with a "cut-out" to permit access to the Maintenance and Control assembly when the door is closed. Spring contacts attached to the Maintenance and Control assembly mate with the door when it is closed to provide RFI protection.

The cabinet is equipped with two blower assemblies which force air from an opening in the cabinet base through a perforated panel in the cabinet top. One blower is mounted at the bottom of each rack.

4.6 CABLE SIMULATOR

A Cable Simulator was designed and developed with the objective of providing a test device which duplicates the specified cable characteristics of a V-(2)-LTA* balanced twisted pair, video cable for cable lengths from zero to seven miles in half mile increments.

* NOTE

The digit appearing in the parenthesis indicates the number of individual transmission lines contained in a given cable assembly.

The Cable Simulator was used in all laboratory testing of Data Modems, Control Logic, and Data Link systems.

The Cable Simulator duplicates the following characteristics of a V-(2)-LTA cable over a frequency range from 50 to 400 kilohertz:

- Characteristic impedance.
- Attenuation.
- Time Delay.

The cable simulator is housed in an RFI tight box. The front panel has input and output connectors and appropriate test jacks. Fourteen switches are provided to permit simulation of up to 7 miles of cable in one-half mile increments.

SECTION 5

DATA LINK SUBSYSTEM DESIGN

The design of the Data Link equipment was performed in parallel. That is to say that the design tasks were divided according to major subassemblies and the design efforts proceeded simultaneously.

The following portions of this section are concerned with the design of the major Data Link components. A large portion of the text is concerned with the design philosophies embraced during the program. The intent is to disclose why certain design approaches were adopted and thereby provide a basis for proper evaluation of program results.

5.1 DATA MODEM

5.1.1 Design Philosophy

5.1.1.1 Major Considerations

In general, the transmission of data over video transmission line is restricted to two factors. They are the cable characteristics and the interference or noise environment. The most important cable characteristics affecting data transmission are phase delay and attenuation. Noise environments that can compromise accurate data transmission include power-line signals, random noise, static, impulse noise, crosstalk, or any combination of these interferences.

5.1.1.2 Diphase Modulation

Diphase modulation, a form of phase modulation, offers the best known compromise between energy spectral occupancy, insensitivity to signal amplitude fluctuations, and noise immunity.

The diphase technique is a modulation method which permits the application of digital techniques. Modulation is accomplished by changing the phase of a square wave every time a mark or "ONE" is transmitted as presented in figure 4-1. No phase change represents a space or "ZERO". The resultant waveform is called digital diphase. The relative phase of the diphase signal contains the message information. The signal is then filtered before transmission over the cable to remove the undesirable high frequency energy. The resultant waveform is called modified diphase. This filtering provides a significant saving in bandwidth with essentially no loss of information. A series of "ZEROS" is transmitted as a 250 kilohertz sine wave, while a series of "ONES" has a fundamental frequency of 125 kilohertz and a third harmonic of 375 kilohertz.

5.1.1.3 Bandwidth

As previously disclosed, the modified diphase signal is generated in the Modem Modulator by passing digital diphase signals through a low-pass filter. The upper cut-off frequency (-3 db point) of the filter employed is 400 kilohertz and was selected in order to pass the third harmonic of the "ONE" bit waveform.

In the Modem Demodulator which receives modified diphase signals a band-pass filter is employed. In general, the application of a band-pass filter is desirable in order to avoid the adverse effects of noise outside of the frequency band associated with the received information. The actual center band frequency of the band-pass filter is dictated by the system data rate. Appropriate selection of filter bandwidth, however, involves a compromise between several incompatibilities. For maximum noise rejection and minimum effects of cable attenuation it is desirable to use a very narrow bandwidth. The reason that narrow bandwidth will minimize cable attenuation effects is that the higher frequencies which are attenuated the most by the cable will be rejected,

and the signal detection networks will only be required to detect the larger amplitude signals near the center-band frequency. If the bandwidth is too narrow, however, the performance of the system will be adversly effected by bit waveform distortion and bit pattern sensitivity. The band-pass filter selected for use in the demodulator has an upper cut-off frequency of 400 kilohertz and a low cut-off frequency of 50 kilohertz.

5.1.1.4 Modulation Error

The Control Logic portion of the Data Link system employs a two-dimensional parity checking scheme to permit the detection of bit errors. This scheme involves the generation of odd parity for each of the Data Link word characters. This is called horizontal parity. Vertical odd parity is then generated over corresponding bits in each character.

It was decided to implement an additional error detection scheme by detecting diphase signal modulation error. The reasons for using this additional error detection were:

- The two dimensional parity scheme implemented in the Control Logic will not detect certain patterns of bit error pairs.
- If one assumes that White Gaussian or random noise will generate random bit errors, the Control Logic parity scheme will achieve the undetected error rate contract requirements. This assumption, however, is actually a "first order approximation." This means that the occurrence of bit error pairs that can defeat the parity scheme may occur more often than the assumption would indicate. Therefore, modulation error detection was implemented to assure compliance with contract requirements.
- The implementation of modulation error detection was a minor design task because of the inherent properties of diphase modulation.

Implementation of modulation error detection is such that modulation errors are detected whenever the last half-bit of one bit and the first half-bit of the next adjacent bit have the same polarity. Figure 5-1 is a timing diagram illustrating the detection of a modulation error.

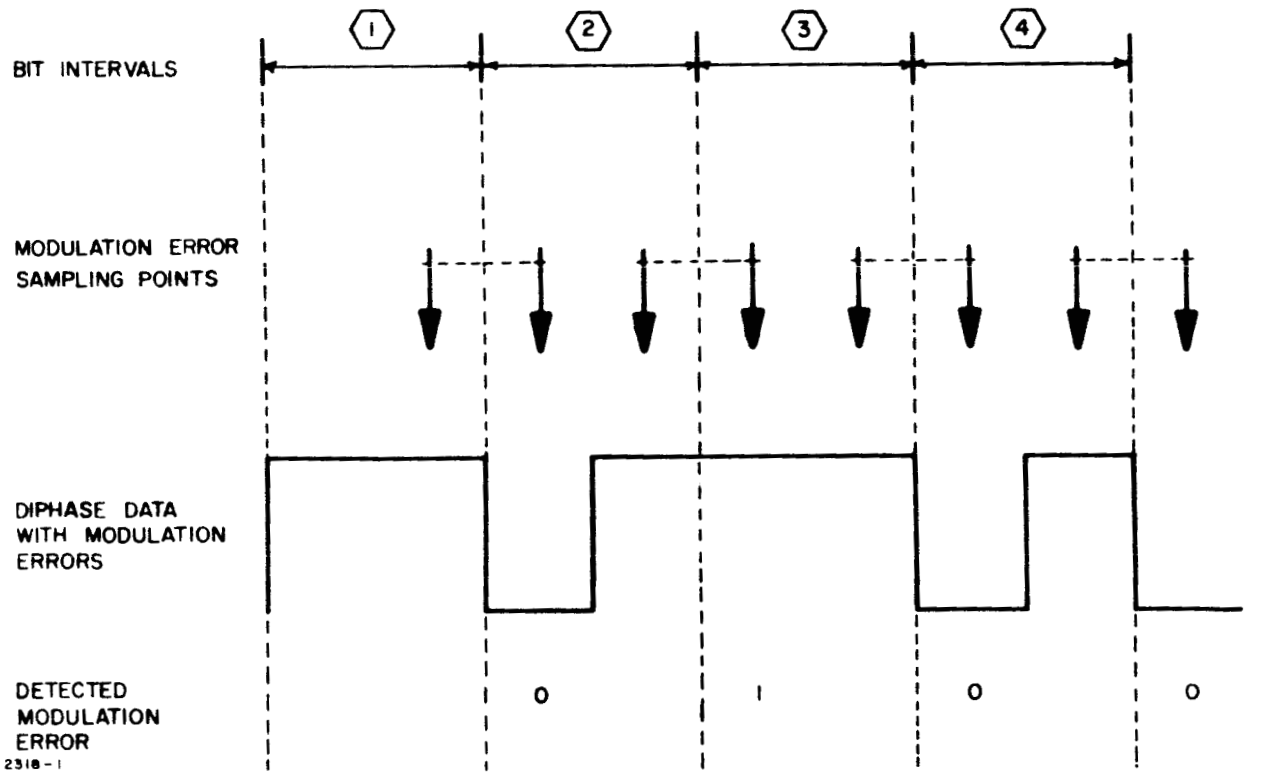


Figure 5-1. Modulation Error Detection Process

5.1.1.5 Data Modem Hardware Design

The approach in the design of the Data Modem was to employ developed and proven hardware common to the Saturn 110 Computer wherever possible. A "worst case" philosophy was used in the design of all special circuits required. This means that all design parameters were considered to simultaneously achieve their worst case extremes in the synthesis and analysis of the circuit. The primary logic design objectives were simplicity, reliability, and timing accuracy. The result was a single nest assembly consisting of 24 printed circuit modules.

Eight new circuit module types were designed for the Data Modem. They are:

- Shielding Board V-118
- Line Amplifier T-052
- Phase Detector T-055
- Input Coupler T-056

- Locked Oscillator T-057
- Master Oscillator T-058
- Cable Equalizer T-059
- Pre-amplifier T-060

A brief description of the eight special modules is presented below:

Shielding Board V-118 - This module is a blank, copper clad, module board with the copper plane connected to signal ground. The board is used in nest slots adjacent to high-impedance, low-level, circuits which may be susceptible to radiated noise.

Line Amplifier T-052 - The design objectives for the line amplifier module were that it should be capable of:

- Accepting digital data from the modulation logic.
- Converting digital to a modified diphase signal.
- Amplifying it to +26 dbm for transmission over balanced video cable.
- Maintaining protection from common mode and differential transients on the cable.

These objectives were met by employing a typical gate input stage, two switched driver stages, and a complementary pair output stage. The output stage is followed by a low-pass filter which limits the energy on the cable to frequencies less than 500 kilohertz (kHz) (3 db down). A balanced output is provided by a wideband isolation transformer. Voltage protection is provided for common mode or differential voltages up to 500 volts on the output of the module.

Phase Detector T-055 - The phase detector T-055, was designed to operate in a phase-locked loop with the locked oscillator T-057 (see Figure 5-2). The output of the phase detector is a dc error voltage with a magnitude proportional to the phase difference of the locked oscillator signal and the average zero crossings of the digital diphase signal.

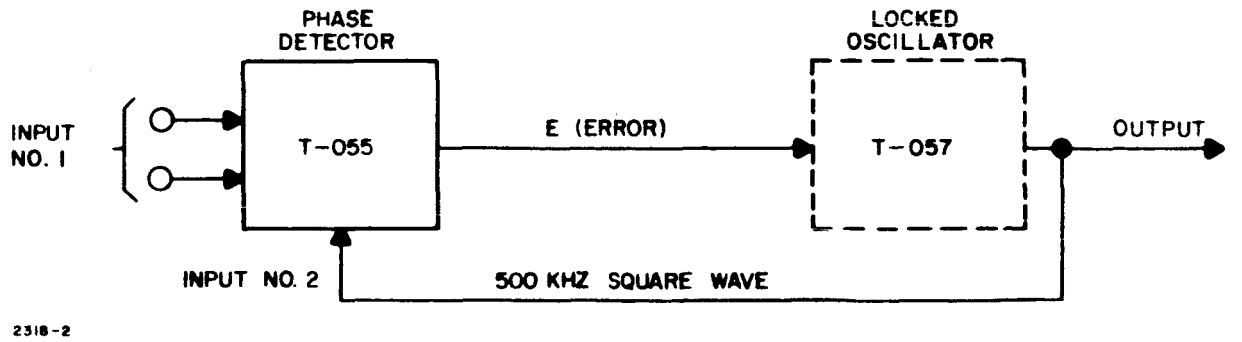


Figure 5-2. Phase-Locked Loop, Block Diagram

The phase detector requires two inputs. One input consists of two signals, a digital diphase waveform and its complement. The zero crossings of the signals produce pulses which are impressed upon the phase detection circuit. The second input is the 500 kHz square wave from the oscillator which is to be phase-locked. A triangular ramp is derived from this square wave. The triangular wave is delayed in time to allow its zero crossings to occur with the zero crossings of the diphase waveforms. This signal is also applied to the phase detection circuit where it is compared with the pulses produced from input 1, resulting in a dc error voltage E, proportional to the phase difference, being generated. This error voltage is used to correct the frequency/phase of the locked oscillator to that of the diphase signal. The phase detector utilizes self-biasing peak detectors to provide high degree of noise immunity.

Input Coupler T-056 - As the design objective, the input coupler was required to convert the modified diphase signal into two complementary digital diphase outputs. These outputs were required to drive the demodulator logic and the phase detector in the locked timer.

The input coupler was required to accept a dynamic input range of ±15 db. This extreme range was accommodated by designing the unit to provide satisfactory performance at the minimum signal level and using clipping diodes on the input to prevent over-loading effects at the higher input levels. It was necessary to match these input diodes due to symmetry requirements of the module output. Tests, over the dynamic

range of the coupler, show the combined mark-space and complementary asymmetry to be less than 150 nanoseconds.

Locked Oscillator T-057 - The locked oscillator was designed to operate in conjunction with the phase detector to form a phase-locked loop, (see Figure 5-2). The output is a 500 kHz square wave locked in phase to the 250 kHz diphase input signal. The design objectives for the locked oscillator were derived from the overall system requirements. Tests on the locked oscillator demonstrated excellent basic stability (1 part in 10^5 for short and long term without over control) and a short lock-in time (less than 1 second).

Master Oscillator T-058 - The master oscillator is a free running stabilized crystal oscillator generating a 500 kHz square wave output. The master oscillator provides the timing for the modem and the data terminal. Frequency stability of the master oscillator was designed to be better than 1 part in 10^5.

Cable Equalizer T-059 - The design objective of the cable equalizer module was that it should be capable of:

- Accepting a modified diphase signal from a balanced video cable over distances from 0 to 7 miles.
- Equalizing the attenuation versus frequency.
- Equalizing time delay versus frequency.
- Providing a constant output for any line length.
- Maintaining protection from common mode and differential transients on the cable.

The cable equalizer module designed to meet these objectives consists of an input transformer, a selectable equalizer section, and a selectable attenuator section. For operational convenience, the equalization and attenuation controls are ganged and adjustable in one mile steps from 0 to 7 miles to fit the specific characteristics of V-(2) -LTA video pair cable. The input to the boards includes a pair of Slo-Blo fuses for high voltage protection. The constants for the equalizer were chosen in a manner to provide equalization of both attenuation and time delay over the frequency range from 50 kHz to 400 kHz when used with V-(2) -LTA cable.

Preamplifier T-060 - The preamplifier module was required to meet the following design objectives:

- Raise the signal level from the cable equalizer T-059 sufficiently to drive the input coupler module T-056.
- Provide band limiting to eliminate extraneous noise and crosstalk outside the band of interest.

The final designed unit has a gain of 34 db ±2.1 db and a passband of 50 to 400 kHz (3 db points).

5.1.2 Data Modem Performance

5.1.2.1 Calculated Performance

Figure 5-3 shows two performance curves. One is the theoretical calculated diphase bit error rate versus signal-to-Gaussian noise ratio. The other represents the worst case performance permitted by RCA internal specification 2184859.

The calculation of the theoretical error rate performance is based on the theoretical bit error rate. The theoretical bit error rate for modified diphase gives the probability of error, neglecting threshold effects, as:

$$Pbe = Pm\left[1 - \operatorname{erf}\left(\frac{2\sqrt{2fo}}{\sqrt{B(9+Pm)}}\sqrt{\frac{\overline{E}}{No}}\right)\right] + (1 - Pm)\left[1 - \operatorname{erf}\left(\frac{3\sqrt{fo}}{\sqrt{B\,(9+Pm)}}\sqrt{\frac{\overline{E}}{No}}\right)\right]$$

Where: Pm = probability of Marks; assumed to be 0.5 for arbitrary messages.

B = noise bandwidth of the Modem band-pass filter; calculated to be 348.5×10^3 cps.

$\overline{E}$ = average energy per bit; in watts per bit.

No = noise power density; in watts per cps.

fo = bit rate; 250×10^3 bits per second.

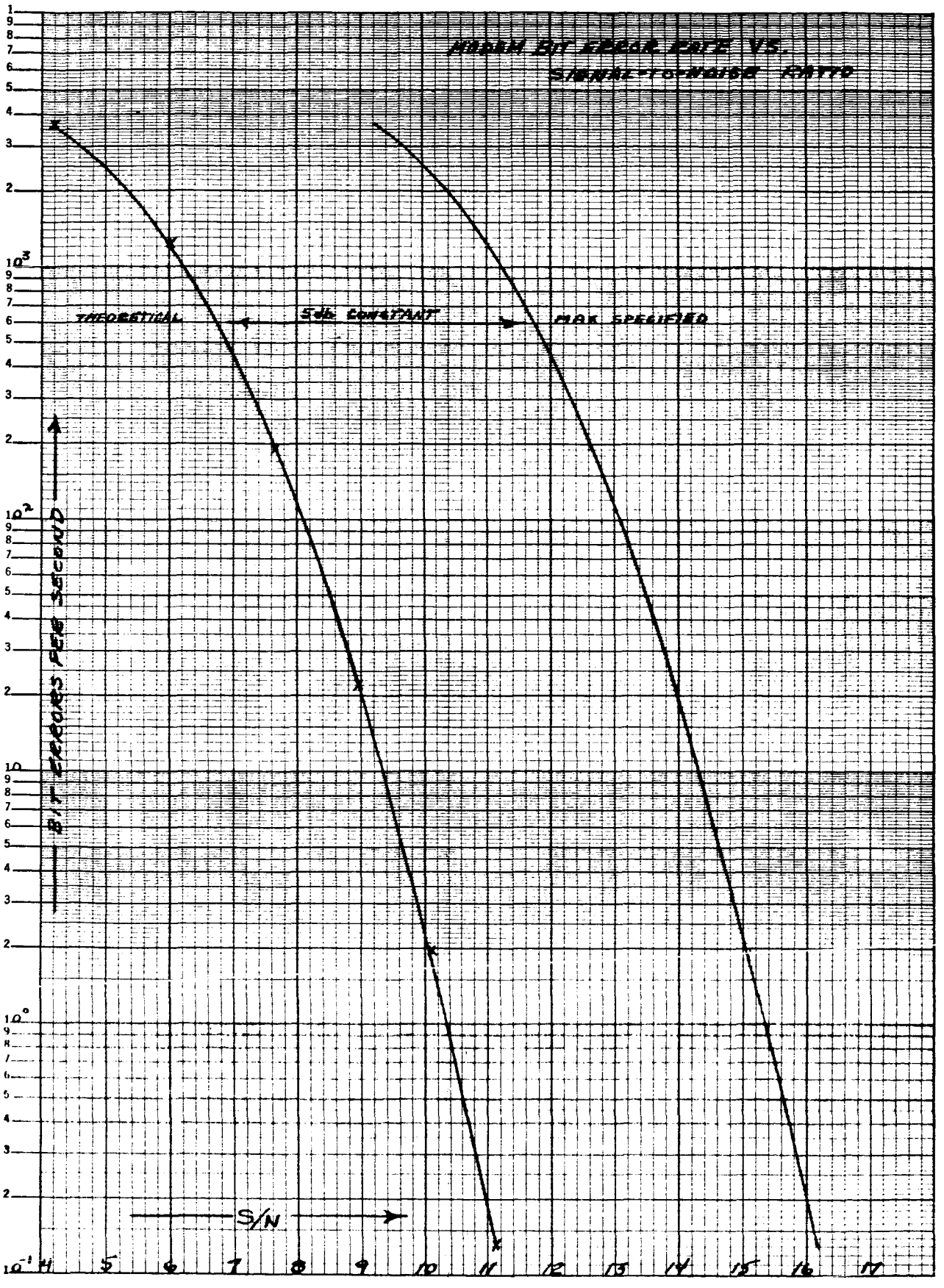


Figure 5-3. Modem Bit Error Rate Versus Signal-to-Noise Ratio

The signal-to-noise ratio is measured at the Modem band-pass filter output. The signal-to-noise ratio (S/N) at that point in the system is related to $\overline{E}$/No at the input to the filter by

$$\overline{E}/No = (S/N)\ (B/fo)\ (1/G)$$

Where:

S/N = signal-to-noise ratio at the band-pass filter output.

G = average midband gain of the filter; calculated to be 0.9.

Therefore:

$$\overline{E}/No = S/N + 1.9 \text{ db.}$$

The theoretical bit error rate versus $\overline{E}$/No was calculated and converted to errors per second versus S/N as shown in the following table. The result is the theoretical curve of figure 5-3.

TABLE 5-1
MEASURED SIGNAL-TO-NOISE RATIO VS BIT ERROR RATE

S/N db	$\overline{E}$/No db (S/N + 1.9 db)	Pbe	Errors/Sec (Pbe X 2.5 X 10^5)
4.22	6.02	1.46×10^{-2}	3.65×10^{3}
6.06	7.96	5.00×10^{-3}	1.25×10^{3}
7.64	9.54	7.69×10^{-4}	1.92×10^{2}
8.98	10.88	8.95×10^{-5}	2.24×10
10.14	12.04	7.85×10^{-6}	1.96
11.16	13.06	5.21×10^{-7}	1.31×10^{-1}

5.1.2.2 Measured Performance

5.1.2.2.1 Bit Error Rate Versus Signal-To-Noise Ratio. - A large number of laboratory tests have been conducted on Data Modem assemblies to measure the bit error rate performance. One has been selected as a standard test for all production assemblies. This test involves connecting the modulator output to the demodulator input through a

Cable Simulator. The Cable Simulator is set at 7 miles. The received signal amplitude in decibels is measured with a true RMS voltmeter connected between test point F on the T-060 module board in nest slot number 3 and the ground bus. White Gaussian noise is injected into the Data Modem between ground and test point M on the T-059 module board in nest slot number 1. Measurement of the noise level in decibels is performed with the RMS voltmeter and with test point L of the V-130 module board in nest slot number 23 grounded. The signal-to-noise ratio in decibels is the difference between the noise level measurement and the signal level measurement.

A test bit pattern is generated and supplied to the modulator. The pattern received at the demodulator output is then compared with the original pattern to establish a bit error rate.

The test bit pattern selected is a 31 bit, pseudo-random, binary code. The bit pattern is:

0000011100100010101111011010011

Note that all combinations of ONES and ZEROS that can occur in a five bit pattern, which is the length of Data Link word characters, except 11111 are present in the test pattern. Because of this characteristic, the pattern shown above was selected as the standard test pattern.

Tests conducted on the first four production Data Modem assemblies in the manner described above disclosed that the bit error rate varied between 127 and 192 bit errors per second for a signal-to-noise ratio of 10 db. This represents an approximate 2.5 decibel deviation in signal-to-noise ratio from the theoretical characteristic. Design specifications for the Data Modem permit a 5 db deviation.

5.1.2.2.2 Bit Error Rate Versus Cable Length. - Tests were conducted to establish the relative performance of the Data Modem as a function of cable length. The Cable Simulator and Modem Cable Equalizer were adjusted for various cable lengths and measurements taken. Test data is shown in Table 5-2. Noted that the measurements include worst case "misadjustments" between cable length and Cable Equalizer settings that would occur in actual operation.

TABLE 5-2
BIT ERROR RATE VERSUS CABLE LENGTH

CABLE SIMULATOR SETTING IN MILES	MODEM CABLE EQUALIZER SETTING IN MILES	SIGNAL-TO-NOISE RATIO IN DECIBELS	BIT ERROR RATE IN ERRORS/ SECOND
0.0	0	10	40.8
0.5	0	10	62.0
0.5	1	10	45.0
1.0	1	10	50.0
1.5	1	10	104.0
1.5	2	10	34.0
2.0	2	10	52.0
2.5	2	10	88.0
2.5	3	10	56.4
3.0	3	10	63.0
3.5	3	10	143.0
3.5	4	10	64.0
4.0	4	10	79.0
4.5	4	10	98.0
4.5	5	10	62.0
5.0	5	10	83.0
5.5	5	10	120.0
5.5	6	10	93.0
6.0	6	10	111.0
6.5	6	10	178.0
6.5	7	10	145.0
7.0	7	10	175.0

5.1.2.2.3 Bit Pattern Sensitivity. - Tests were conducted for bit pattern sensitivity in the manner outlined in Paragraph 5.1.2.2.1. The standard 31 bit test pattern was employed as well as patterns consisting of all ONES and all ZEROS. The objective was to determine the characteristics of Data Modem bit pattern sensitivity. The results obtained are tabulated in Table 5-3.

Several general observations can be made concerning the bit pattern sensitivity data. First, the 31 bit test pattern produces a larger bit error rate for a given cable length and signal-to-noise ratio than either the all ZERO or all ONE pattern. This condition supports the belief that the standard test pattern produces results that may be representative of actual Data Link system operation and not "best-case" performance.

Note that the all ONE pattern produces a lower error rate than the all ZERO pattern for a given cable length and signal-to-noise ratio. If one wishes to hold the noise level constant, however, the indication is that the ONE pattern will produce less errors. For example, consider operation at 7 miles, signal-to-noise ratio of 8 db, and all ZERO pattern. The data indicates a bit error rate of 248 bits per second. If the pattern is changed to all ONES, the signal-to-noise ratio would change to 10.3 db because of the increase in signal level by 2.3 db. By extrapolation using the error rates for all ONE patterns at 7 miles and 8 db and 10 db signal-to-noise ratios, the bit error rate would decrease to approximately 40 bits per second. The change in bit error rate when changing the ONE and ZERO content of bit patterns was experienced during laboratory test and evaluation of the entire Data Link system as reference described in Paragraph 5.2.2.2.1.

5.1.2.2.4 Testing with V10-LTA Cable. - Data Modem tests were conducted at the Marshall Space Flight Center in Huntsville, Alabama to assure satisfactory Data Modem operation with an actual cable installation. The tests verified the Data Modem performance obtained by using the Cable Simulator.

The cable used was V10-LTA. The number 10 in the designation means that the cable contains ten video pairs of transmission lines. Cable lengths available for the tests were 2, 4, and 6 miles. There were no other signals on the cable during Data Modem tests.

TABLE 5-3.
DATA MODEM BIT PATTERN SENSITIVITY

SIMULATOR SETTING	PATTERN	SIGNAL LEVEL db	NOISE LEVEL db	SIGNAL/NOISE RATIO db	ERRORS/SEC.
0	Test	-8.0	-18	10	115
0	Zero	-8.3	-18.3	10	25
0	One	-7.5	-17.5	10	104
5	Test	-8.4	-18.4	10	84
5	Zero	-8.9	-18.9	10	19
5	One	-7.3	-17.3	10	80
7	Test	-8.2	-18.2	10	144
7	Zero	-9.2	-19.2	10	21
7	One	-6.9	-16.9	10	59
0	Test	-8.0	-16	8	759
0	Zero	-8.3	-16.3	8	320
0	One	-7.5	-15.5	8	814
5	Test	-8.4	-16.4	8	732
5	Zero	-8.9	-16.9	8	260
5	One	-7.3	-15.3	8	714
7	Test	-8.2	-16.2	8	948
7	Zero	-9.2	-17.2	8	248
7	One	-6.9	-14.9	8	593

The test conducted with the cable was similar to that described in Paragraph 5.1.2.2.1 except that the cable was used rather than the Cable Simulator. The noise level on the cable during the test was so low that bit errors could not be detected. White Gaussian noise was injected into the Data Modem as described in Paragraph 5.1.2.2.1 in order to obtain measurable bit error rates. The tests were conducted at a 10 db signal-to-noise ratio and were duplicated with a Cable Simulator to provide comparison data. The obtained data is listed in Table 5-4. Note that the error rates for the cable and for the Cable Simulator are in remarkably close agreement for 2 and 4 mile lengths. Cable Simulator application caused a larger bit error rate for the 6 mile length. Various other measurements during the test effort disclosed that the signal delay for the cable at the 6 mile length was 1.5 microseconds less than the published nominal cable delay and Cable Simulator delay.

TABLE 5-4
ERROR RATE WITH V10-LTA CABLE
WHITE GAUSSIAN NOISE INJECTION
FOR 10 db S/N LEVEL

CABLE LENGTH	AVERAGE BIT ERRORS/SECOND USING VT10-LTA CABLE	AVERAGE BIT ERRORS/SECOND USING CABLE SIMULATOR
2	64	66
4	71	73
6	68	110

5.2 CONTROL LOGIC

5.2.1 Design Philosophy

5.2.1.1 Major Considerations

During the design phase of the Data Link Control Logic, the major figures of merit for system performance were considered to be information transfer rate and undetected error rate. Information transfer rate is defined as the time rate of transfer of correct words and the undetected error rate is defined as the time rate of transfer of undetected erroneous words. In general, these two performance parameters are incompatible. In order to determine the optimum compromise between these incompatabilities, a third factor must be specified. This is the noise environment in which the Data Link system would be required to operate.

Definition of the noise environment was an unknown parameter throughout the design phase of the Control Logic. Therefore, the approach was to design for a relatively low undetected error rate at high noise levels and permit the information transfer rate to be dictated by the noise environment encountered at a specific installation.

5.2.1.2 Word Format and Error Detection

The selected Data Link word format is shown in figure 5-4.

Referring to figure 5-4, it is noted that there are twelve parity bits used for error detection. The parity scheme employed provides for an undetected word error rate of 2.8×10^{-14} words/word for a random bit error rate of 10^{-4} bits/bit. The bit transmission rate is 250 kilobits/sec. These numbers were reflected in RCA proposals and contract requirements.

It is important to note at this time that contract requirements are for a White Gaussian noise environment resulting in a 10^{-4} single bit error rate. If it is assumed that the Gaussian noise will generate perfect random bit errors, the parity scheme employed will achieve this performance level. This assumption is a good approximation for

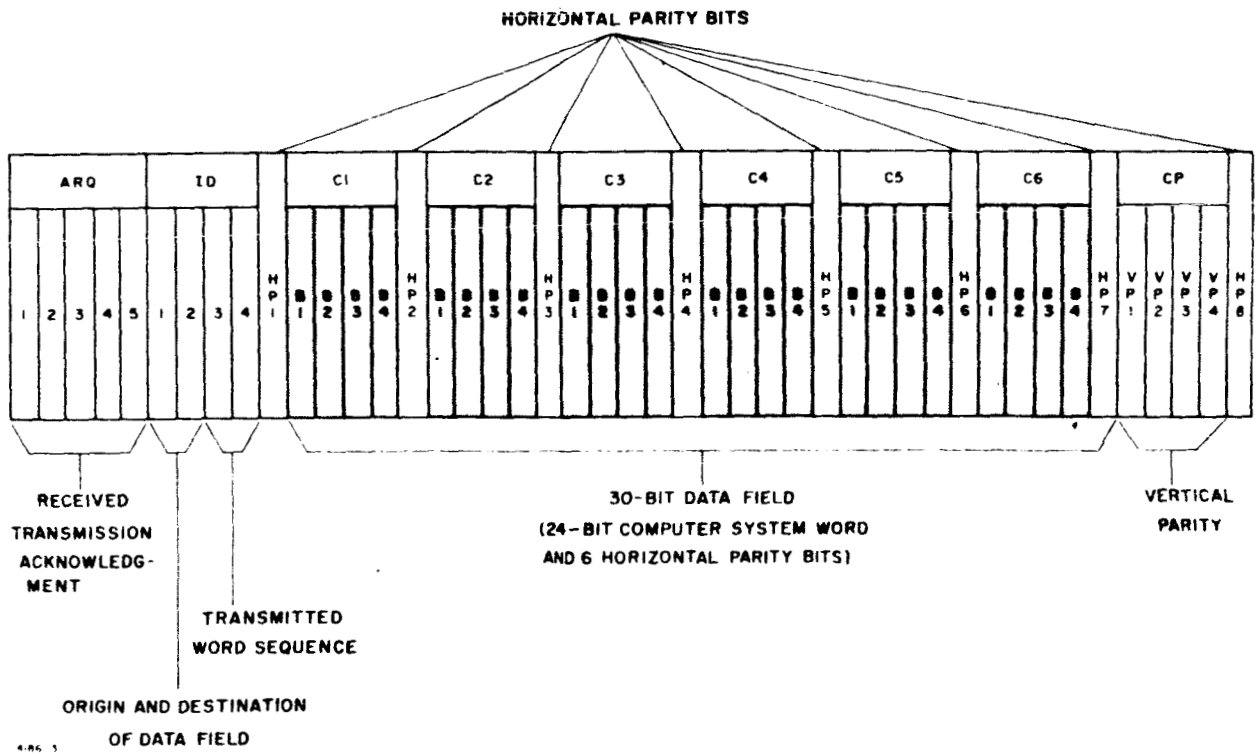


Figure 5-4. Data Link Word Format

the system considered. The fact that in general it is an approximation can be illustrated in a qualitative sense by simply letting the bit time approach zero. Noise "spikes" which modify single bits for large bit times will begin to modify adjacent bits as the bit time decreases, thus destroying the random single bit error approximation. The fact that random or Gaussian noise does not guarantee random bit errors was in part the reason for utilizing an additional error detection scheme in the system. This additional protection is described as the Modem modulation error detection scheme.

5.2.1.3 ARQ Character

The ARQ character (automatic repeat request) provides the stimulus for correction of erroneous words. If a received word is found to be in error, then the Data Link

terminal that transmitted the word is requested to retransmit by means of the ARQ character.

The ARQ character coding is such that a binary code 10011 is transmitted to indicate that there is no request for retransmission. A 01100 code is a transmitted repeat request. A Data Link terminal receiving an ARQ character interprets any code other than 10011 as a repeat request. This criteria was established when considering the noise modification of ARQ characters. Since a detected error results in a retransmission, any modification of the code 10011 results in a retransmission.

5.2.1.4 System Word Timing

A timing diagram illustrating the system word timing is shown in Figure 5-5. In this figure, the ARQ character received in response to a transmitted word is received during the word time following the transmitted word. However, response to the ARQ character does not take place until the second word time following the transmitted word. In the example illustrated in Figure 5-5, the Slave Terminal receives erroneous word A. The resulting repeat request is received at the Master Terminal during the next word time, word time 2, and word A is retransmitted during word time 3. In order to maintain correct word transmission sequence, all words following a retransmitted word must be retransmitted in proper sequence until a no repeat request ARQ is received for the retransmitted word. All words received following an erroneous word must be ignored until the word is correctly received.

A primary objective in the design of the Data Link Control Logic and Data Link system in general was to reduce the word time delay between the end of a transmitted word and receipt of the associated ARQ character. In a word repeat system which requires preservation of transmitted word sequence, this time delay greatly influences the information transfer rate in a noise environment. For example, if this delay was 1.5 word times it would require 4 word times to correctly transfer one word of information in the event of a single retransmission. A second reason that it is desirable to minimize the delay between the end of a transmitted word and receipt of the ARQ

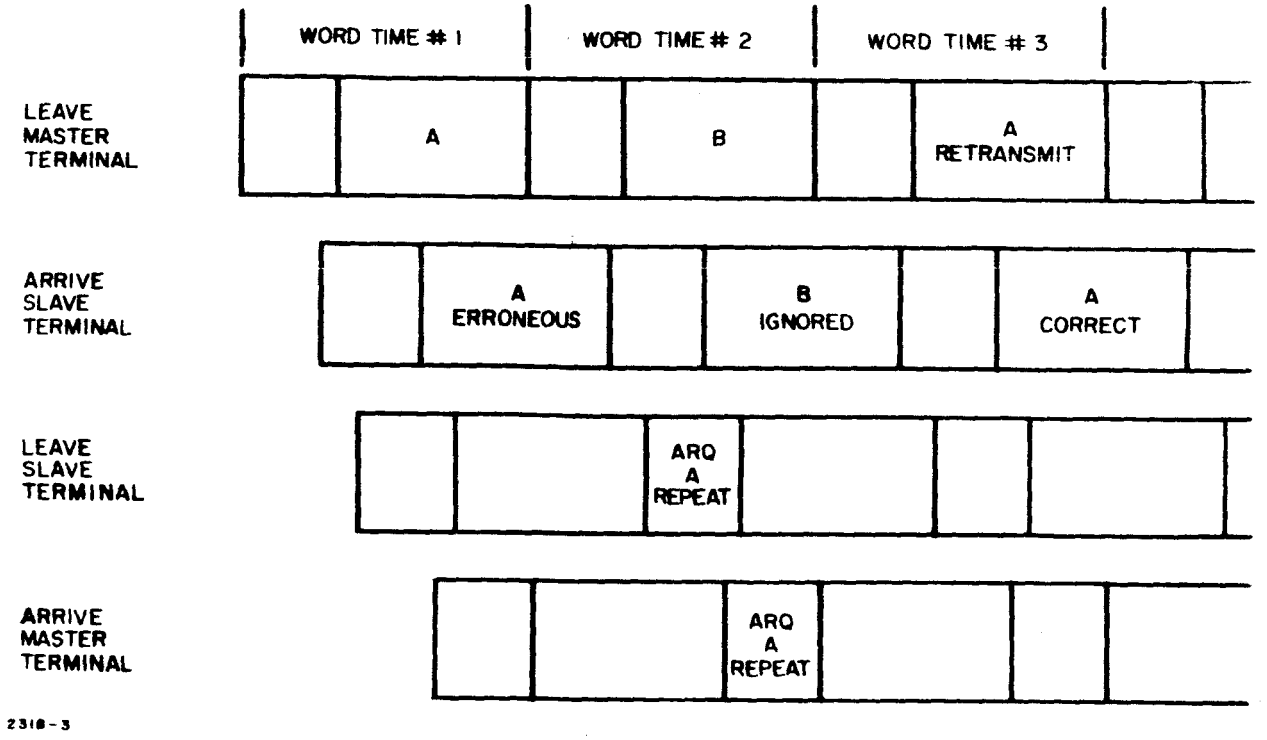


Figure 5-5. Word Timing Diagram

character is that the storage or memory capacity required for words that may require retransmission is reduced. In the Data Link Control Logic the retransmission storage register has a capacity for two words. Had the delay been 1.5 word times, a three word capacity would have been required. A reduction in the hardware required to implement a system generally improves the predicted system reliability with respect to random hardware failures.

The optimum condition is achieved when the delay time is less than a single word time. The reason is that a word may not be found to be erroneous until after it is completely received, thereby causing the ARQ character to be generated and transmitted during the following word time. This optimum condition was achieved in the Data Link design by reducing all data propagation and processing delays in the equipment consistant with good design practice. The major contribution was made in the Modem design by minimizing electronic filter delays.

5.2.1.5 ID Character

In the Data Link word structure, the ID character contains two types of information. The first is the origin and destination of the word. The second is a binary repeat code which indicates word sequence. The code is:

00 - Original word or second word in repeat cycle.

01 - First word in 1st repeat cycle.

10 - First word in 2nd repeat cycle.

11 - First word in 3rd repeat cycle.

The objective of this code is to provide a means by which a terminal receiving data can determine if proper word sequence is maintained, if there is a possibility that information has been lost, and to assess the difficulty of correct information transmission.

5.2.1.6 Synchronization

The Saturn Data Link system must be time synchronized in order to transfer information between the two associated computers. The Control Logic initiates and systematically controls the synchronization process by a series of logical operations known as a "reframing cycle". The ability of the system to maintain synchronization once it is established is a function of the Modem Phase-Locked Oscillator stability. This stability is controlled by specification to be such as to ensure phase lock continuity during and after either the total or partial loss of the incoming diphase signal for a time duration of 200 microseconds.

During Control Logic design certain criteria were established by which the Control Logic could recognize loss of synchronization. These rules are:

- A terminal receives a fourth repeat request for the same word.
- A terminal determines that the same word is erroneous for the fourth time.

- A terminal receives a word with a "sync" word ID code which indicates that the other terminal is in a reframing cycle.
- It has been determined that a word has been retransmitted erroneously. The implication is that a malfunction has occurred in the retransmission storage equipment and therefore information has been lost.
- A received word has an ID repeat code numerically smaller than expected which indicates that information has been lost.

In general, these conditions establish that the system will resynchronize whenever the Control Logic determines that there is a possibility that information has been lost or that there is a degree of difficulty in transferring information between Data Link terminals. In some respects these conditions are artificial in that some may be satisfied without the actual loss of time synchronization between the Modem Phase-Locked Oscillator and the master timing source. If time synchronization is lost, however, one or more of the Control Logic conditions will be satisfied.

When actual time synchronization is lost, information is lost because of the inability of the receiver portion of the Control Logic to properly interpret received information. The rules for the Control Logic initiating resynchronization include the loss of information condition. For these reasons, whenever resynchronization takes place it must be assumed that a loss of information has occurred.

5.2.1.7 Control Logic Hardware Design

The approach in the design of the Control Logic was to employ developed and proven hardware common to the Saturn 110 Computer main frame hardware. This was accomplished resulting in a four nest assembly implemented with 96 Saturn printed circuit modules. There were no special circuits designed for Control Logic application.

However, one unique application of standard circuits was required. This was the effective electrical paralleling of -6.5 volt output clamp diodes on line drivers used

to generate signals to the IODC. This configuration is shown on RCA 2173068 logic diagram DL7. The cathodes of diodes on V-032 modules are connected to the outputs of V-129 line driver circuits. The common anode sides are connected to -6.5 VDC. This causes a diode on the V-032 module to be electrically connected in parallel with the output -6.5 VDC clamp diode of each V-129 circuit. The reason for this configuration is to prevent "over-stress" of V-129 output diodes when the Data Link cabinet power is off and IODC power is on. The output impedance of the Data Link -6.5 VDC bus is less than one ohm when the power is off. This condition permits a relatively large current to flow through the output clamp diode to the IODC. The paralleling of diodes does not guarantee any division of current through the diodes but does restrict the maximum power dissipation of either of the parallelled diodes. A detailed analysis of this condition was published on 1 October 1964 in response to Saturn Reliability Program Action Request Log No. 13.

5.2.2 Control Logic and System Performance

5.2.2.1 Calculated Performance

Following are a series of curves which describe the performance characteristics of the control logic. Because of the strong dependence of system performance on Control Logic characteristics, they also represent system performance.

The curves are calculated performance characteristics. Certain assumptions have been made to simplify the calculations. They are:

- Noise injection on the video cable generates perfect random bit errors.
- For system performance which employs two Data Link terminals the bit errors generated on each of the two video transmission lines are equal and independent.
- For the bit error rates considered, the probability of a conversion of a repeat request, 01100, to a no repeat request, 10011, is negligible.

- There are no retransmission register parity errors. This assumption is based on the fact that retransmission register parity errors would be caused by an equipment malfunction.
- There are no parity errors for information transfer between the Data Link terminal and the IODC.
- The IODC is always available to accept data when data is to be transferred to it from the Data Link terminal. In actual operation if the IODC is not available, the receiving terminal generates a repeat request and system resynchronization may result.
- It is assumed that the actual time required in the synchronization process is negligable. Actually at low bit error rates the time required is less than ten word times. At high bit error rates the time is longer because bit errors will interfere with the synchronization process.

A detailed outline of the calculations may be found in the Appendix.

Following are definitions of parameters reflected in Figures 5-6 through 5-11. The common independent variable for all curves is Pb = average bit errors in bit per bit.

Figure 5-6

Pw = average word errors in word per word.

λ Bit = average bit errors in bit per second.

λ Word = average word errors in word per second.

Figure 5-7

t = average word information transfer rate in microseconds and in word times.

Figure 5-8

T sync = average terminal available time which is the time between re-framing cycles in seconds and microseconds. The curves are for word

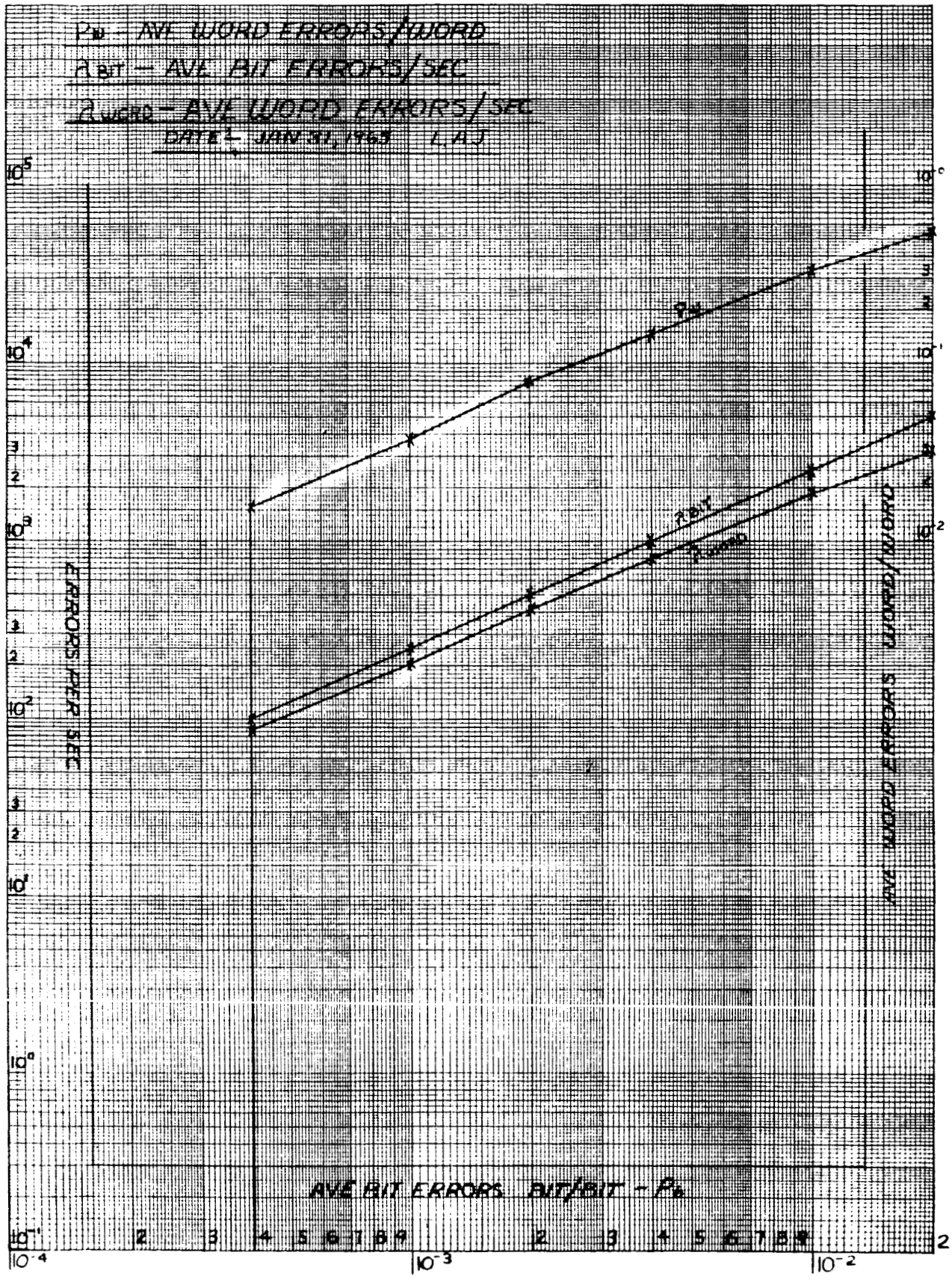


Figure 5-6. Average Word Error Rates

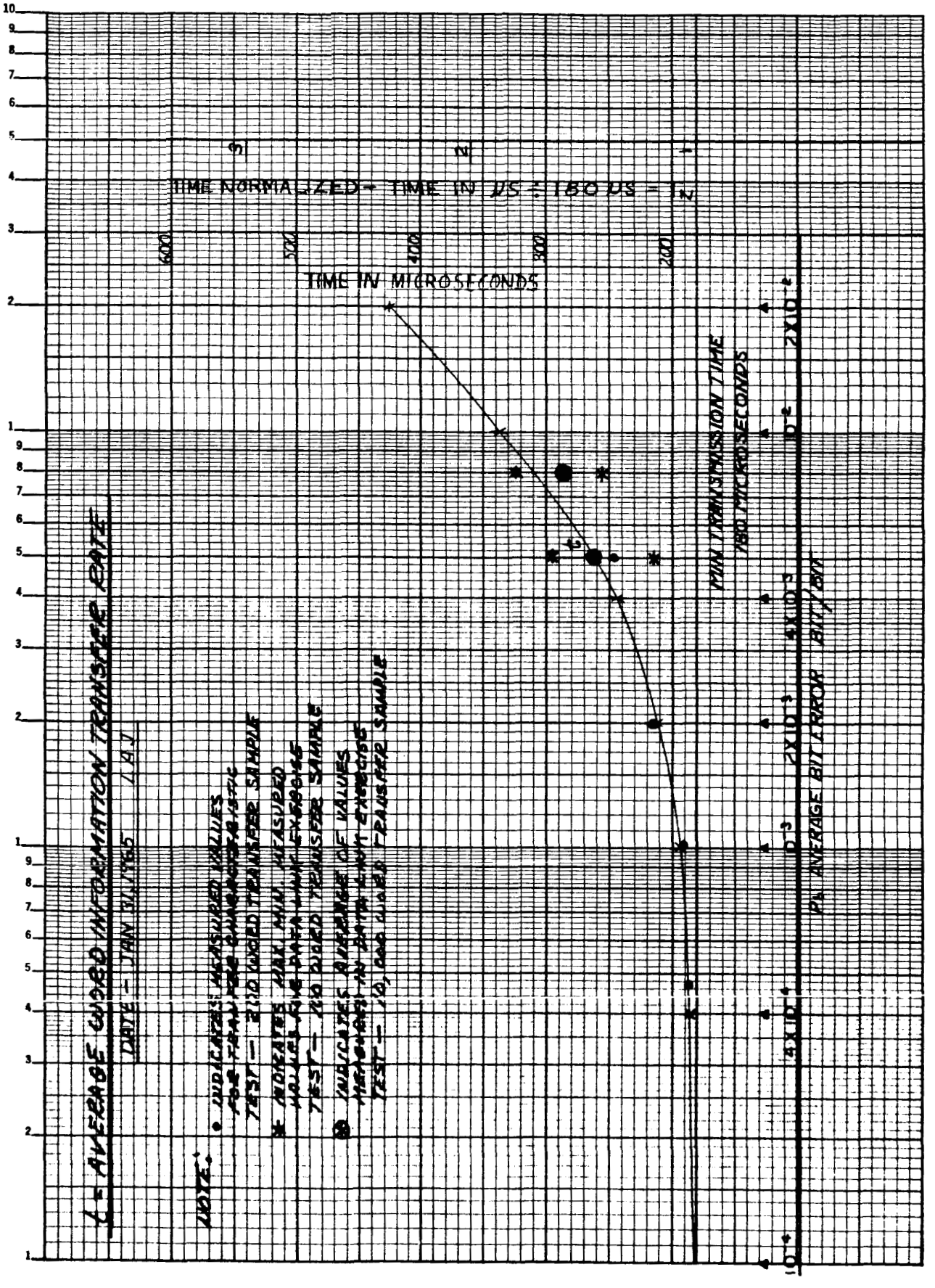


Figure 5-7. Average Word Information Transfer Rate

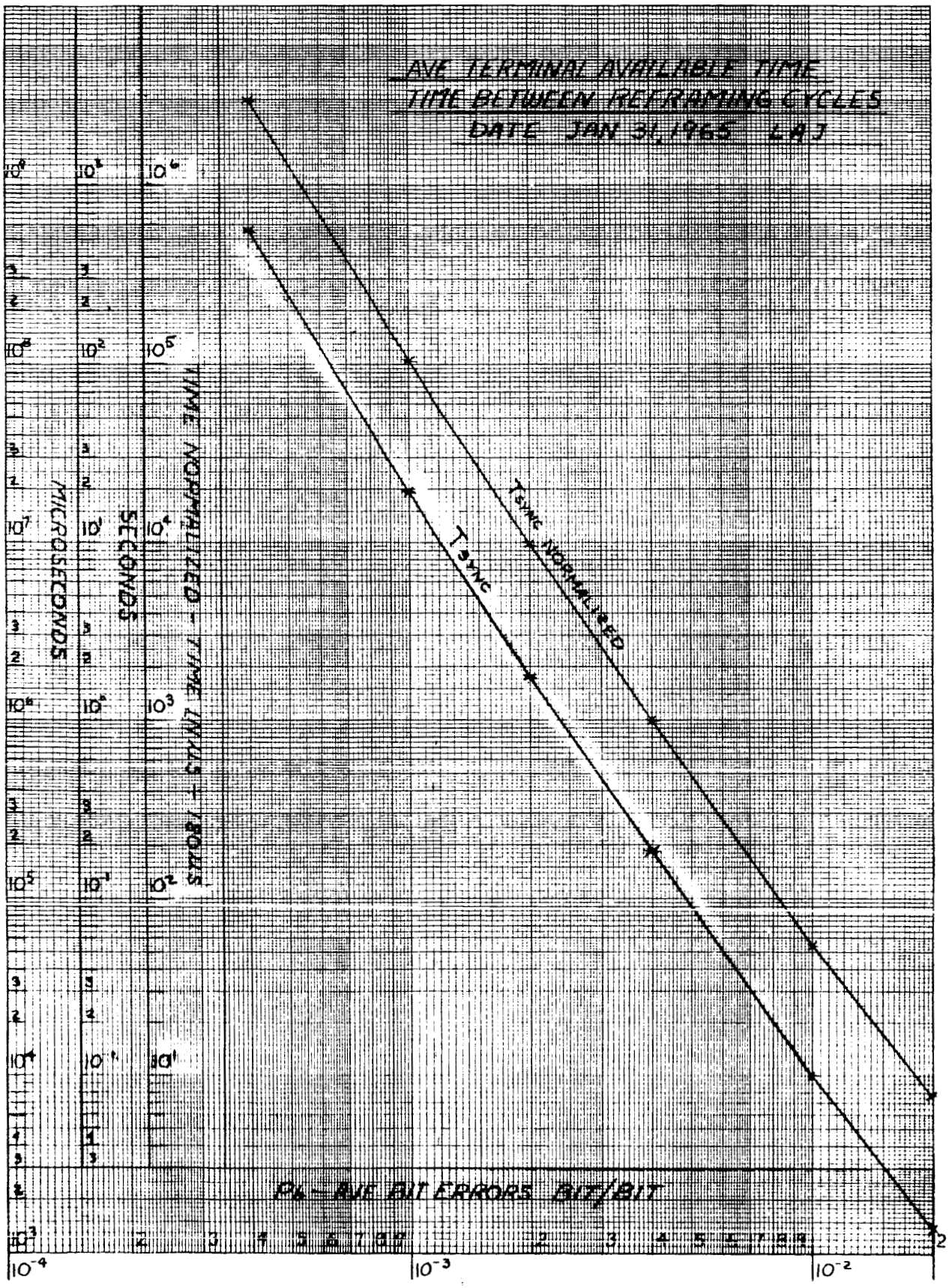


Figure 5-8. Average Terminal Time Available Between Reframing Cycles

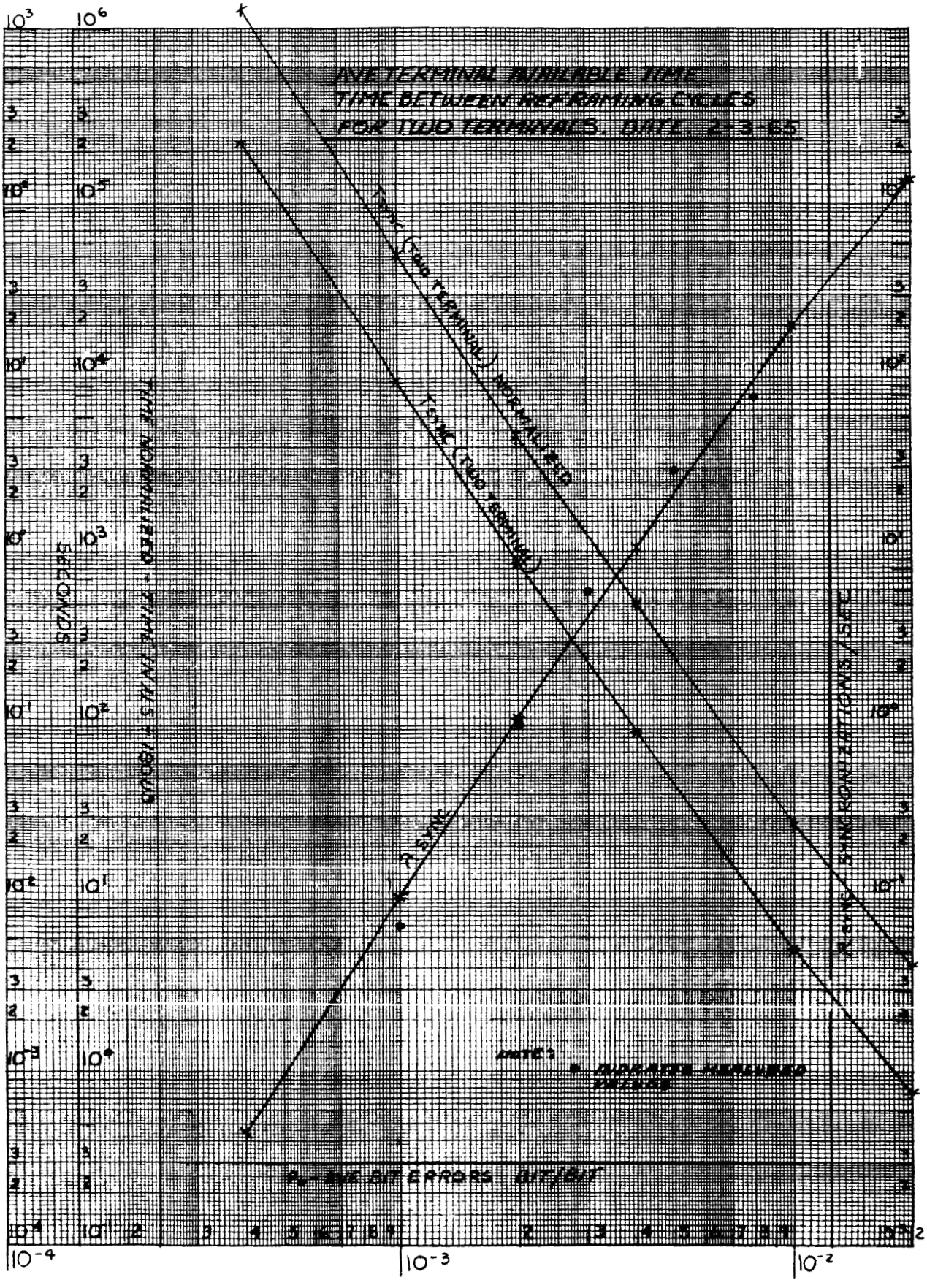


Figure 5-9. Average Terminal Time Available Between Reframing Cycles for Two Terminals

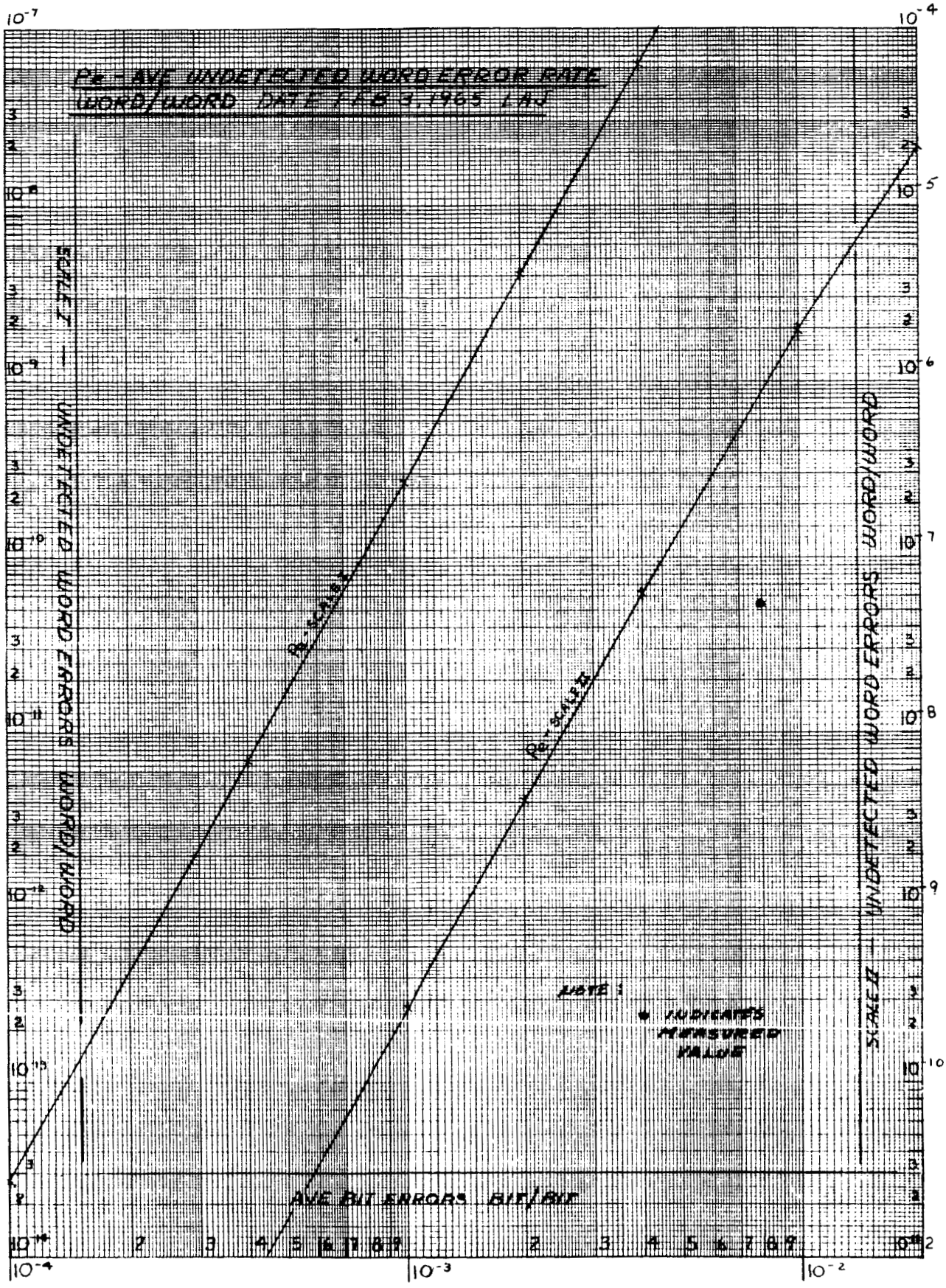


Figure 5-10. Average Undetected Word Error Rate

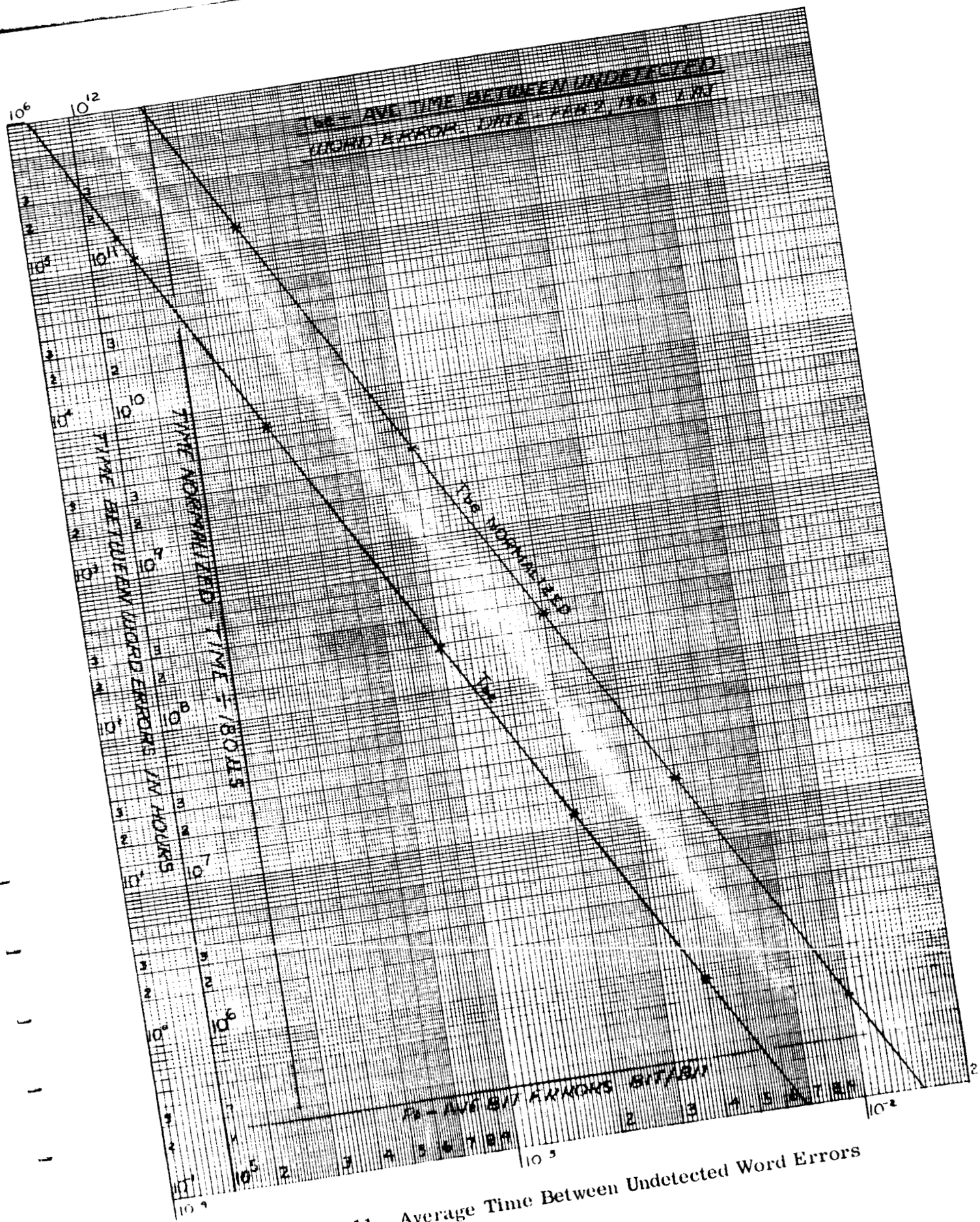


Figure 5-11. Average Time Between Undetected Word Errors

errors influencing a single terminal which is equivalent to bit error generation on only one of the two video transmission lines between two Data Link terminals.

T sync normalized = average terminal available time which is the time between reframing cycles in word transmission times. The curve is for bit error influence on a single terminal.

Figure 5-9

T sync (two terminal) = average terminal available time which is the time between Reframing Cycles in seconds. The curve is for two terminals with bit errors generated on each of the two video transmission lines which are random, equal, and independent.

T sync (two terminal) normalized = average terminal available which is the time between reframing cycles in word transmission times. The curve is for two terminals with bit errors generated on each of the two video transmission lines which are random, equal, and independent.

λ sync. = average synchronization rate in synchronizations per second. This curve is the reciprocal of T sync (two terminal).

Figure 5-10

Pe = average undetected word error rate in word per word. This curve reflects performance characteristics of the Control Logic in that the only error detection capability considered is parity checking. Actual system undetected error rates will also depend on the detection of modulation errors by the Data Modem.

Figure 5-11

Tbe = average time between undetected word errors in hours.

Tbe normalized = average time between undetected word errors in word transmission times.

5.2.2.2 Measured Performance

5.2.2.2.1 Average Word Information Transfer Rate.- In Figure 5-7, the results of two performance tests are shown. One of these tests was a transfer Characteristic Test (Ref. NSI-532-1, paragraph 6.4.8.5). This test involves the transfer of 100 words in both directions between two Data Link terminals. Each test therefore involves the sampling of 200 word transfers. The test is controlled by computer program. The time required to transfer the 100 words in each direction is measured and recorded by the computer. Four tests were performed; each at a different bit error rate. Each test data point shown in figure 5-7 for the transfer characteristic test is the average transfer word time for 200 word transfers. The second test performed was the Data Link Exercise Test (Ref. NSI 532-1, paragraph 6.4.6). Results of this test are also shown in figure 5-7. This test is similar to the Transfer Characteristic Test except that the 100 word transfer time in each direction is measured once every 100,000 word two-way transfers. Each test conducted involved 50 samplings of two-way 100 word transfers which is the same as 100 samplings of 100 word transfers or 10,000 single word transfers. Two complete tests were conducted. One at an average bit error rate of 5×10^{-3} bit per bit and the other at 8×10^{-3} bit per bit. The data shown for these tests are the maximum and minimum average word times for a 100 word transfer and average word times for the entire test or 10,000 word transfers.

There are two known possible explanations for the deviation of measured values from the calculated characteristic. They are:

- The size of the sample was not sufficient to establish a true statistical average.
- Influence of bit pattern sensitivity in the Data Modem signal-to-noise ratio versus bit error rate characteristic. Refer to Paragraph 5.1.2.2.3.

In each Data Link Exercise Test a total of five million two-way word transfers was affected. The noise injection level was adjusted to provide the desired bit error rate

and not readjusted after the original set-up. The word information content was a number which was continually incremented thereby causing the ONE and ZERO bit content of words to change. Because of the change in signal level to bit pattern, and therefore signal-to-noise ratio and bit error rate, the initially established bit error rate may not be the appropriate abscissa point at which to reference the test results.

5.2.2.2.2 Synchronization Rate.- Results of synchronization rate measurements are shown in figure 5-9. White Gaussian noise was injected into the Data Modems of a Data Link test system. The noise level was adjusted to achieve the desired bit error rate. The procedure is described in NSI 532-1, section 6.1.4. The synchronization rate was measured with an electronic counter connected to control logic nest location 412-L.

5.2.2.2.3 Undetected Word Error Rate.- A computer controlled test was conducted for the purpose of detecting the transfer of an erroneous word via the Data Link system. Results of this test are shown in Figure 5-10. The bit error rate established was 8×10^{-3} bit per bit which corresponds to a 1.5 kilocycle per second word error rate. One erroneous word was undetected after the transfer of 17.1 million words. This is an undetected word error rate less than that predicted by the calculated undetected error rate characteristic.

Although it is not possible to draw a conclusion from this single sample, it is possible that this desirable deviation is caused by the Data Modem modulation error detection scheme which was not considered in the calculated characteristic.

The direct measurement of undetected errors is impractical because of the long time duration required for such a test. This is the result of the low undetected rate expected. Therefore, it is necessary to determine the undetected error rate indirectly by a combined analytical and emperical approach.

NASA representatives from Bellcomm Inc. proposed a method of evaluation which accelerates the generation of undetected errors and also avoids the assumption that individual bit errors occur independently.

The procedure involves inhibiting the vertical parity checking networks so that vertical parity would always seem to be satisfied. This would accelerate the occurrence of undetected errors. An undetected error would then occur whenever there were an even number of bit errors in a five bit word character thereby causing horizontal parity to be satisfied. The procedure would then be to measure the undetected error rate resulting from White Gaussian noise injection at a bit error rate low enough to assure that virtually all of the undetected word errors would be the result of only two bit errors per character. The calculation of the actual undetected error rate with vertical parity checking activated would be:

$Pe = 28 \sum_{i=1}^{10} \left(\frac{ni}{n} \right)^2$ undetected word errors per word transmitted where:

- The summation is from 1 to 10 because there are 10 ways in which two bit errors may occur in a character.
- n is the total number of characters.
- ni is the number of accepted errors with the i th error pattern.

A test was conducted to evaluate the difference between the Bellcomm undetected error rate and the characteristic of figure 5-10. This test involved the transfer of 900,000 words at an average bit error rate of 7.4×10^{-4} bit per bit. The Data Modem modulation error and vertical parity networks were inhibited. The calculated undetected error rate by the Bellcomm method was 10 per cent higher than the value dictated by the characteristic of figure 5-10.

5.2.2.2.4 Effectiveness of Modulation Error Detection. - Two laboratory tests were conducted to determine the merit of using both a modulation error and parity error detection scheme. A test was conducted in which 300,000 words were transferred with a bit error rate of approximately 10^{-3} bit per bit. First only the horizontal parity checking network was enabled and then the test was repeated with only the modulation error network enabled. There were 26 undetected errors with only horizontal parity

checking activated and 15 undetected errors with only the modulation error activated. From this test it appears that modulation error detection is more effective than the horizontal parity checking scheme.

Another test was conducted in which 900,000 words were transferred at an average bit error rate of 7.4×10^{-4} bit per bit with both the modulation error and horizontal parity error activated. The test was repeated with only the horizontal parity networks activated. Undetected error rates calculated for the two conditions were 2.91×10^{-11} and 8.82×10^{-11} undetected word errors per word respectively. This indicates that the undetected error rate was reduced by a factor of 2.8 when modulation error detection was employed.

5.2.3 Recommendations

Following is an outline of recommendations concerning possible changes in the Control Logic which may improve system performance. These recommendations are based on experience gained during the execution of the contract.

5.2.3.1 Information Transfer Rate

In actual operation at relatively high bit error rates, the average information transfer rate is more adversely effected by the synchronization rate then by the word retransmission rate. The reason is that T sync becomes small and once the system goes into synchronization one must assume that words have been lost. This means that if synchronization takes place during a block transfer of data that the entire block of data will have to be retransmitted.

In all of the testing performed during the design and development of the Data Link system, synchronization has never occurred because of a loss of synchronization between the Data Modem phase-locked oscillators and the master free-running oscillator. This is probably due to the high degree of stability achieved in the Locked Timer design. In every case, synchronization has occurred because of the criteria outlined in Paragraph 5.2.1.6 of this report.

In the event that "field operation" discloses a need to increase the information transfer rate under high noise conditions, certain changes may be made in the criteria for synchronization. Specifically, increase the number of times a word may be retransmitted before synchronization is initiated. In order to do this and at the same time preserve the Data Link word length of 45 bits, the present repeat code philosophy would have to be abandoned. Another philosophy which could be adopted would be to tag each word transmitted with a sequence code. In this case, only two bits (as in the repeat code) would be required to provide the capability of detecting out of sequence, unnecessary, and correct retransmissions.

Another method for increasing information transfer rate would be by decreasing the length of the present Data Link word. This could be done by degrading the undetected error rate presently achieved. It is believed that the horizontal parity checking scheme could be eliminated and still achieve the undetected error rate performance reflected in figure 5-10. This is because the modulation error scheme appears to have a higher capability for preventing undetected errors than the horizontal parity checking scheme. Elimination of horizontal parity would decrease the Data Link word length by 25 per cent.

5.2.3.2 Tactical Programming Aid

At the present time there is no "hardware" means for notifying the computer when a command word has been lost in transmission. There are several ways that this condition can be detected by proper programming. However, in order to simplify the programming it is recommended that a "Command Word Transmission Busy" (XCTB) signal be generated by the Data Link Terminal. This signal would notify the computer via the IODC that transmission is in progress but acceptance of the word by the remote terminal has not occurred. After executing a command word instruction the computer would not execute another instruction until XCTB is reset or until after synchronization has occurred.

5.3 MAINTENANCE AND CONTROL ASSEMBLY

The Data Link Maintenance and Control Assembly was designed to provide a direct interface between Data Link equipment and system operating personnel. The assembly permits ON-LINE system monitoring and TEST or off-line monitoring and control.

During design of the Maintenance and Control assembly, the primary objective was to provide versatility. The unit was not designed to provide a specific capability or to permit the solution of specific problems. The reason for this approach is that the anticipated utility would depend on equipment and system status and the immediate objectives of operating personnel. These factors could not be adequately assessed and specified during the equipment design. Therefore, the approach was to provide versatility. Optimum use of the Maintenance and Control assembly depends to a large degree on a thorough understanding of the Data Link equipment and Data Link system operation. To illustrate this point, consider the illumination of the MODULATION ERROR indicator. The significance of such an alarm would be different if the Data Link terminal was in actual on-line system operation than if one were attempting to verify operability of a single Data Link terminal with the modem modulator output connected to the demodulator input. For the on-line case, the alarm may be the result of a power-off condition or malfunction in the remote terminal. For single unit test the alarm may indicate a malfunction in the Data Modem assembly.

Various Maintenance and Control assembly operating procedures may be generated depending on the desired objective. The Saturn Data Link Terminal Instruction Manual contains a procedure which may be used for verifying the operability of the Data Modem and Control Logic assemblies. Refer to table 5-5 of the Instruction Manual.

5.4 POWER SYSTEM

5.4.1 Design Philosophy

During the design phase of the Data Link power system, the following requirements were established.

- Sequencing of DC voltages required by the Modem and Control Logic circuits shall be provided.

- Over and under voltage detection shall be established at a level sufficient to protect the circuits from voltage levels that could be destructive.
- Sufficient operational control interlocks shall be provided to protect the equipment from accidental operator error. In the event that the DC POWER ON and DC POWER OFF controls are activated simultaneously the power OFF condition shall prevail.
- Sufficient controls shall be provided for disconnecting the power system from the Data Modem and Control Logic circuits for the purpose of maintenance and calibration.

5.4.1.1 Power Supplies

The DC voltages required for proper operation of the Data Link circuits are +26 VDC ±3%, -26 VDC ±3%, and -6.5 VDC ±3%. A single power supply, capable of generating the required voltages, was selected. RCA Specification Control Drawing 2184570-2 defines the unit for Saturn S1B systems and 2185545 for Saturn SV systems. The operational properties of the 2185545 unit are identical to those of 2184570-2. The differences are primarily in workmanship requirements and component quality control requirements.

The selection of the power supply for Data Link applications was based on several factors. First, the unit could satisfy all Data Link power requirements. The unit will generate any one of the three required voltages. Transient response is good, and the variation in DC output voltage is not expected to exceed ±1.5% thereby providing adequate margins for adjustment and power distribution voltage drops. Secondly, the unit was specified for application in the SIB Dual Displays systems developed for NASA under contract NAS 8-5433. This, together with the fact that the single power supply type could fulfill all Data Link DC power requirements, appeared

to offer some obvious advantages when considering computer system maintenance and logistics problems.

5.4.1.2 Sequencer, Power Control

5.4.1.2.1 Voltage Sequencing.- Stated voltage sequencing requirements for the circuit modules used in Data Link require:

ON SEQUENCE	OFF SEQUENCE
-6.5 VDC	+26 VDC
-26 VDC	-26 VDC
+26 VDC	-6.5 VDC

A review of the circuits, most of which are common to other Saturn Computer equipment, disclosed that the sequence time relationship of the +26 volts was not critical from the standpoint of causing catastrophic circuit failures. However, it will cause degradation in circuit performance if the sequence time relationship alone is applied to the circuits. This effect is considered "long term" and is not expected to be detectable until after the +26 volts has been applied for approximately 100 hours. Another disclosure was that it is not necessarily a requirement that each voltage in the sequence reach its steady state value before changing the next voltage in the sequence. In the case of the +26 volts it is only required that the absolute value (26 volts) not be significantly greater than the absolute magnitude of -26 volt at any instant in time. The requirement between the -6.5 volts and -26 volts is that the -26 volts should not exceed -7.5 volts before the -6.5 volt bus has reached a voltage value between zero volts and its normal operating level. The -7.5 volts is dictated by transistor voltage limitations. The requirement for voltage sequencing and thereby the method by which it is implemented is very closely related to the definition of "zero volts". Zero volts may have two meanings. One is that a given power bus has no voltage applied to it by virtue of an open circuit between the bus and the voltage source. This is generally the connotation when one considers dc sequencing in which dc voltages

are switched with contacts to the voltage distribution bus. Another definition of zero volts is that the bus is at ground potential or is connected to ground potential through a moderately low impedance. This is generally the meaning when considering ac sequencing in which the application of dc voltages results from sequencing primary ac power to the power supply inputs. In ac sequencing, however, one is usually faced with the fact that the output impedance of a power supply when it is off is not quantitatively defined.

If dc sequencing was employed for the Data Link equipment, the sequencing relationship between the -6.5 and -26 voltages would have been very critical. This is because -26 volts could be applied to transistors with lower voltage ratings. However, ac sequencing was employed and the impedance of the -6.5 volt bus when the -6.5 volt power supply is off controlled by connecting a one ohm resistance between ground and the -6.5 VDC bus. Refer to figure 5-12. The one ohm resistance serves as a bleeder resistance for the -6.5 volt power supply and is required for the connection configuration employed because load current is required to flow from the -6.5 volt bus rather than into it.

The ohmic value of the bleeder resistance is dictated by certain boundary conditions. The minimum value is limited by the current capacity of the -6.5 volt power supply. The maximum value is limited by the requirement that a -6.5 volt power supply current flows through the resistance to provide voltage regulation.

It can be seen that the configuration implemented relieves the criticality between the -6.5 and -26 volt sequence. Even if the -6.5 volt power supply was removed from the system the voltage on the -6.5 volt bus would be between ground potential and -6.5 volts when the -26 volt supply was on, and the -7.5 volt limitation would not be exceeded.

5.4.1.2.2 Over/Under Voltage Sensor. - The Data Link Sequencer, Power Control assembly is equipped with a self-contained over/under voltage sensor sub-assembly. This unit is primarily used to sense the dc voltages and automatically turn the power

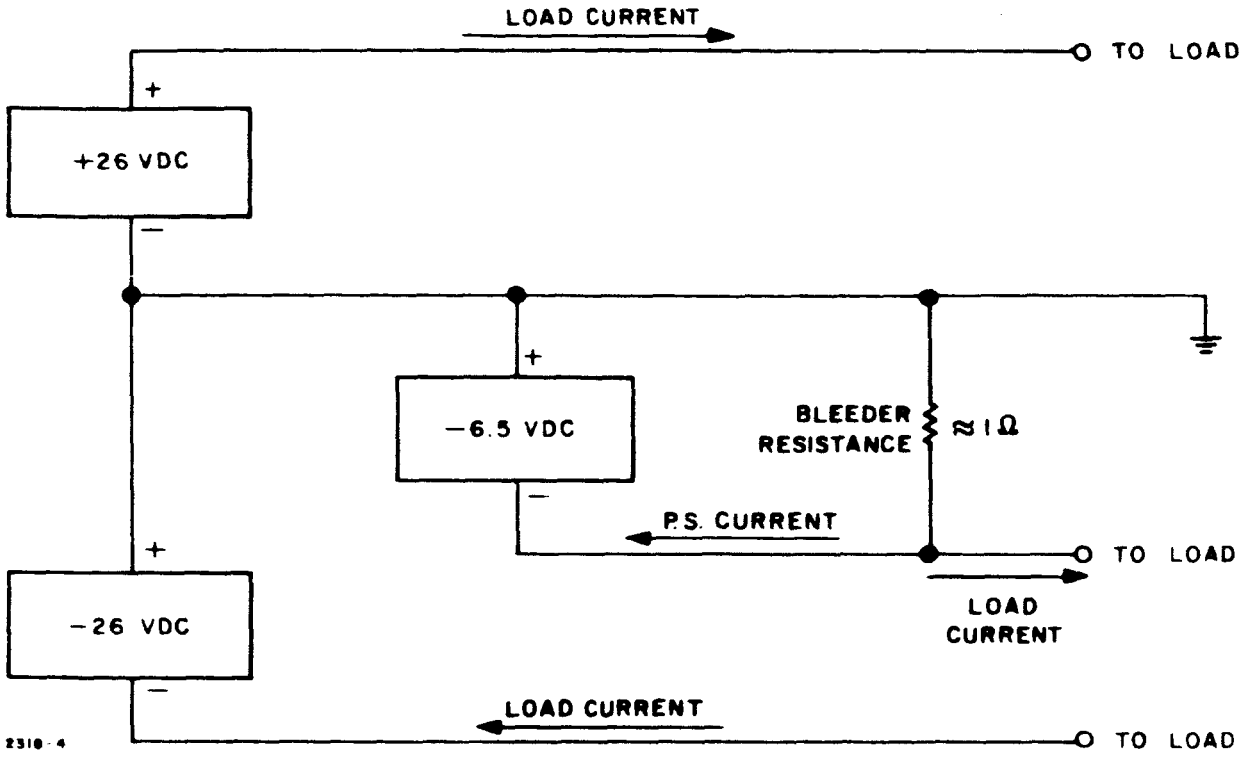


Figure 5-12. Data Link Power Supply Connection Schematic

supplies off when a potentially destructive over or under voltage is detected. Because of the voltage sensing ability, the unit is also the key element in the voltage sequencing operation.

The OVER/UNDER VOLTAGE SENSOR was designed to have adjustable sense voltage threshold levels and adjustable DC test voltages. The implementation of adjustable, self contained, test voltages was done to facilitate testing and maintenance of the equipment.

The over and under voltage threshold levels are calibrated to approximately plus and minus 6 per cent of the nominal power supply voltages. The test voltages permit bench calibration of the unit without requiring the use of power supplies.

The sequencer assembly is equipped with two maintenance controls. They are; the POWER SUPPLY TEST control and the OVER/UNDER VOLTAGE TEST control.

Activation of the POWER SUPPLY TEST control disconnects all power supply voltages from the circuit modules. In all other ways the power system is operational. The OVER/UNDER VOLTAGE TEST control can only be activated when the POWER SUPPLY TEST control is activated. This control causes the internally generated, adjustable, test voltages to be applied to the OVER/UNDER VOLTAGE SENSOR rather than the Data Link power supply voltages. This action permits calibration of the OVER/UNDER VOLTAGE SENSOR while it is completely installed in the sequencer assembly. This calibration would not be possible using the Data Link power supplies because the -26 volt supplies cannot be adjusted to the ±6% limits. The OVER/UNDER VOLTAGE SENSOR test voltages have another utility. Activation of the OVER/UNDER VOLTAGE TEST control provides a means by which the power supplies can be activated for trouble-shooting purposes even though a power supply malfunction has occurred that would otherwise automatically cause them to be turned off.

5.4.2 Measured Performance

5.4.2.1 Voltage Sequencing

Typical dc voltage waveforms for the power on and power off sequence are shown in Figure 5-13.

5.4.2.2 Measured Voltage Distribution Drops

Distribution voltage drops are the difference between the voltage appearing at a module with respect to the ground bus at the module, and the power supply output voltage with respect to the ground bus at the power supply. Measured voltage drops are presented in Table 5-5.

5.4.2.3 Measured Data Link DC Current Requirements

Measured supply output currents are presented in table 5-6.

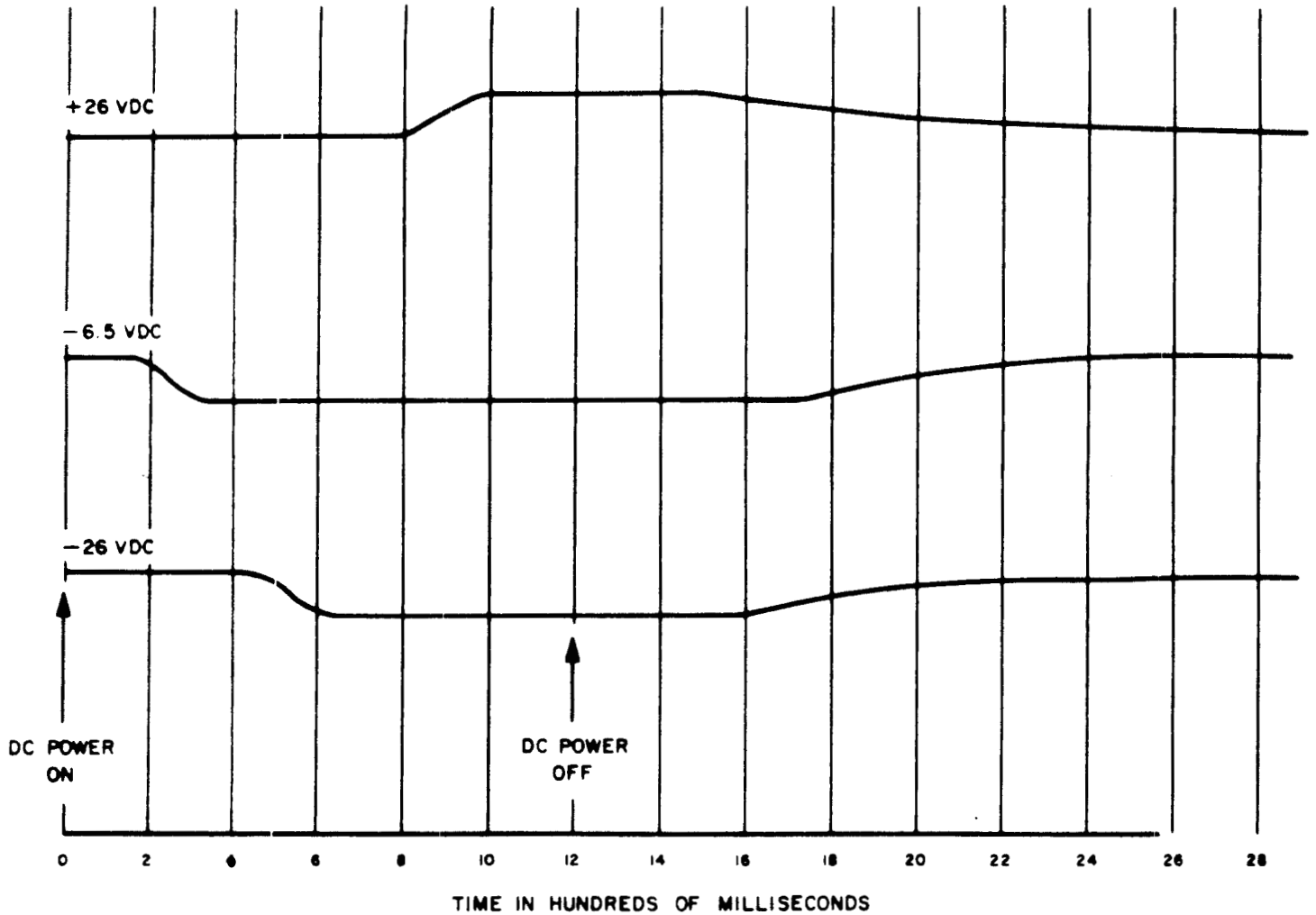


Figure 5-13. Data Link Power ON/OFF Sequence

TABLE 5-5
MEASURED VOLTAGE DISTRIBUTION DROPS

VOLTAGE	VOLTAGE DISTRIBUTION DROP
-6.5 volts dc	53 millivolts dc maximum
-26 volts dc	30 millivolts dc maximum
+26 volts dc	19 millivolts dc maximum

TABLE 5-6
MEASURED POWER SUPPLY OUTPUT CURRENTS

VOLTAGE	CURRENT
-6.5 volts dc	3 amps
-26 volts dc	13 amps
+26 volts dc	4 amps

5.4.2.4 Data Link Terminal Measured Primary Power Requirement

The steady state power requirement for a single Data Link terminal is presented in Table 5-7.

TABLE 5-7
MEASURED PRIMARY POWER REQUIREMENT

VOLTAGE	CURRENT
113 vac, 60 cycle, 1 phase	21.2 amps

5.5 CABINET ASSEMBLY

5.5.1 Design Philosophy

The approach in the cabinet assembly design was to utilize as much hardware common to the rest of the Saturn 110 Computer system as possible. Special purpose mounting

brackets and fixtures were required as well as a unique front door to permit access to the Maintenance and Control assembly. Figure 5-14 shows the location of assemblies within the Data Link cabinet.

All cables connecting to the Data Link Cabinet are shielded assemblies. Special RFI junction boxes were designed for video transmission line connections. The reason for the junction box design was that it was required to terminate the video transmission line shields in an open manner. It was required to have complete ground isolation between the two Data Link terminals in the system.

The cabinet cooling requirement is that localized temperatures inside the cabinet do not exceed 113°F. This requirement results from the fact that all circuits used in the Data Link Cabinet, except possibly those in the power supplies, have been designed to operate in a worst case ambient temperature of 113°F. Considering that the maximum air input temperature may be 80 °F, the maximum temperature rise in the cabinet must not exceed 33 °F.

The design goal, by contract requirement, for insulation between signal and chassis ground, was 200 megohms at 500 volts dc with a R.H. of 30 percent at 25 °C. This degree of isolation was achieved by controlling the insulation resistance of the subassemblies by specification and by insulating mounting hardware from the cabinet.

5.5.2 Measured Performance

5.5.2.1 Cabinet Internal Temperature Rise

Laboratory temperature rise measurements were made on a fully operational Data Link terminal. A list of maximum temperature rise values for various locations in the cabinet is presented in Table 5-8. The temperature rise values are with respect to the laboratory ambient temperature of 72°F. The front of nest locations is defined as the module insertion side of the nest.

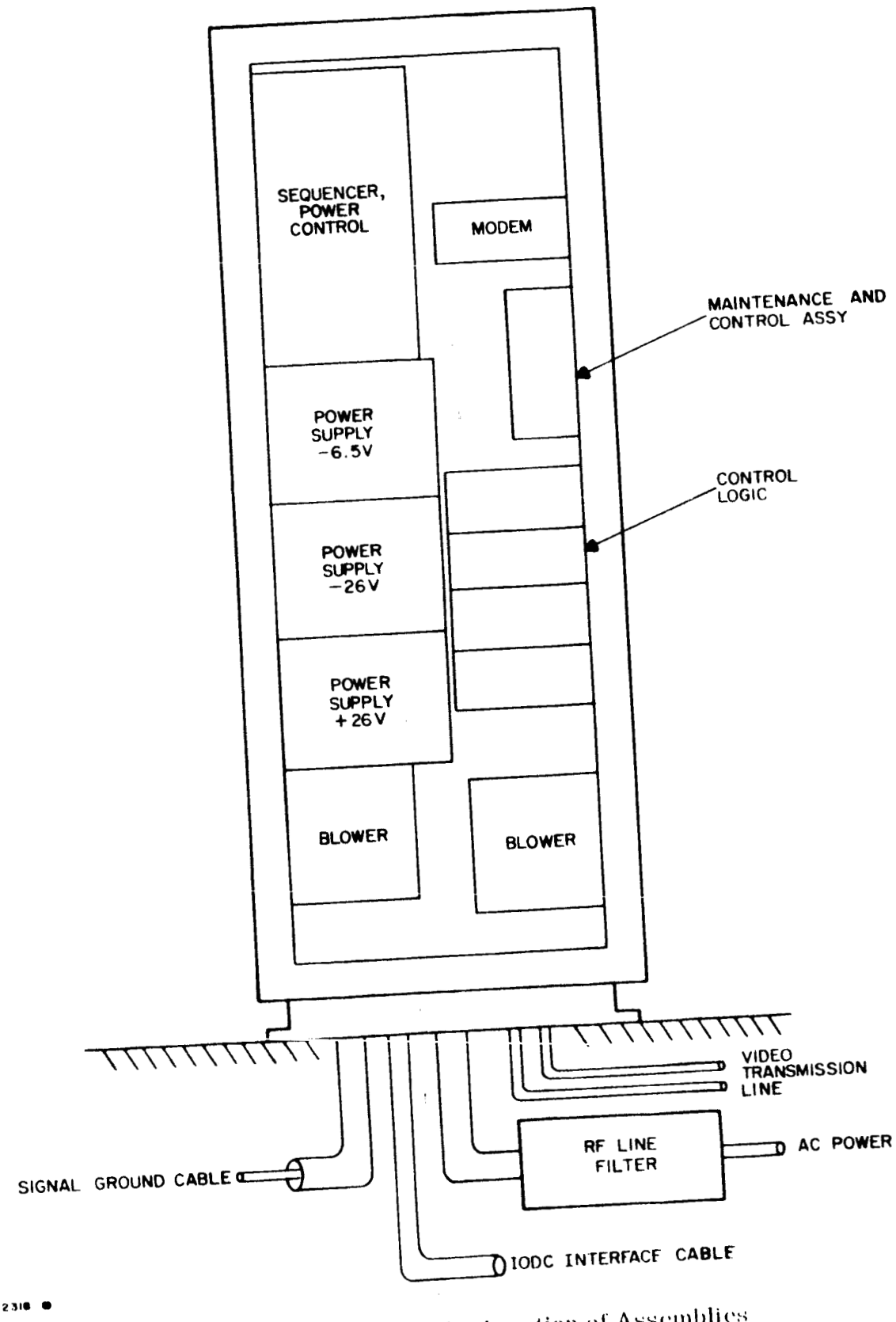


Figure 5-14. Data Link, Location of Assemblies

TABLE 5-8
CABINET INTERNAL TEMPERATURES

LOCATION	MAXIMUM TEMPERATURE RISE (33 F MAXIMUM ALLOWABLE)
Top of cabinet exhaust	12.1 °F
Top of Sequencer, Power Control assembly	12.2 °F
Between Sequencer, Power Control assembly and -6.5 volts dc power supply	15.2 °F
Between -6.5 volt power supply and -26 v power supply	11.6 °F
Between -26 volt power supply and +26 volt power supply	13 °F
Front of Control Logic assembly	20.5° F
Front of Data Modem	14.6 °F
Top of modem assembly	22.6 °F (directly over T-052 module)

5.5.2.2 Insulation Resistance

An insulation measurement was made on a fully equipped Data Link terminal between the signal ground bus and the cabinet. The measured resistance was 399 megohms at 500 volts dc, 48 per cent relative humidity, and 19°C. This is well within the required design goal of 200 megohms.

SECTION 6

DATA LINK RELIABILITY

The Data Link contract states; "The design reliability goal shall be .99 for seven (7) hours of equipment operating time."

During the design and development of the Data Link equipment, there was no single direct action taken to assure attainment of this goal. The general approach was to apply a "worst case" design philosophy. Inherently critical design configurations were avoided at all times. Design reviews were conducted on all new designs. An attempt was made to minimize stress ratios for individual electrical components.

6.1 CALCULATED RELIABILITY

The calculated mean time between failure for a single Data Link terminal is 6,600 hours. This represents a calculated probability for success for 7 hours of operation of .99894. The probability for success, considering both Data Link terminals in a Data Link system, is .99788 for 7 hours.

The above figures account for only "random" failures. They do not take into account failures resulting from marginal performance caused by inadequate design or failures caused by equipment abuse.

6.2 RELIABILITY TESTING

A 1000 hour Data Link reliability test was conducted under laboratory conditions. Two Data Link terminals, serial numbers 030-0001 and 030-0002, were exercised for a period of 1000 hours. The equipment was monitored and tested periodically to

verify performance. At the beginning of the reliability test, the two Data Link terminals had been in operation for periods of 220 and 233 hours respectively.

Following is a summary of the equipment failures during the 1000 hour reliability test:

1. The fuse, F2, of the Sequencer, Power Control assembly of terminal serial number 030-0002 was blown during the replacement of a test jumper connection. This jumper was a special test connection used to sequence the DC power off in the event of an over temperature condition in the cabinet. Normally an audible alarm would sound and the power would remain on. The equipment was required to operate unattended during 1000 hour test, therefore, the test jumper was employed.

2. Test cable W000001 failed due to an open circuit. This cable is only used for single terminal test in which the terminal is disconnected from the actual video transmission lines. This failure would not effect system operation. The test cable was installed in terminal 030-0001.

3. Two indicator lamps in the MODE SELECT switch and DC POWER ON switch were burned out in terminal 030-0001. These indicator lamp failures would not effect system operation. The elapsed operational time of the terminal at the time of these failures was 1111.4 hours.

SECTION 7

PROGRAMMING

Three basic programs were generated for this contract. A short description of each program is contained in paragraphs 7.1 through 7.3.

During the generation of programs for this contract, several programming techniques were discovered that will minimize the probability of programming error. Three recommended techniques are detailed in section 7.4.

7.1 DATA LINK - SPECIAL TEST MODE TEST

The purpose of this test is to provide a controlled analysis of the data link terminal receiver functions.

The test is written to run on a single computer with either a single IODC and terminal or two IODC's and terminals (see Figure 7-1). As the transmitted data comes directly from the computer with no check bits added for error detection, noise inspection is not used for this test.

The test is logically divided into three parts. Each part consists of several series of 24 data link words. Each word sequence will cause a single word to reach the IODC Status Register. If any word sequence fails to give the expected response, the particular sequence will be identified and the erroneous word printed out. When an error occurs, the sequence may be repeated continuously to permit fault isolation within the receiver using conventional test equipment. It should be noted that each acceptable word is followed by a minimum of seven test or all zero words. This insures that the IODC status register will always be available to erroneous command words. Further detail concerning this test plus a program listing is contained in NSI 532-1

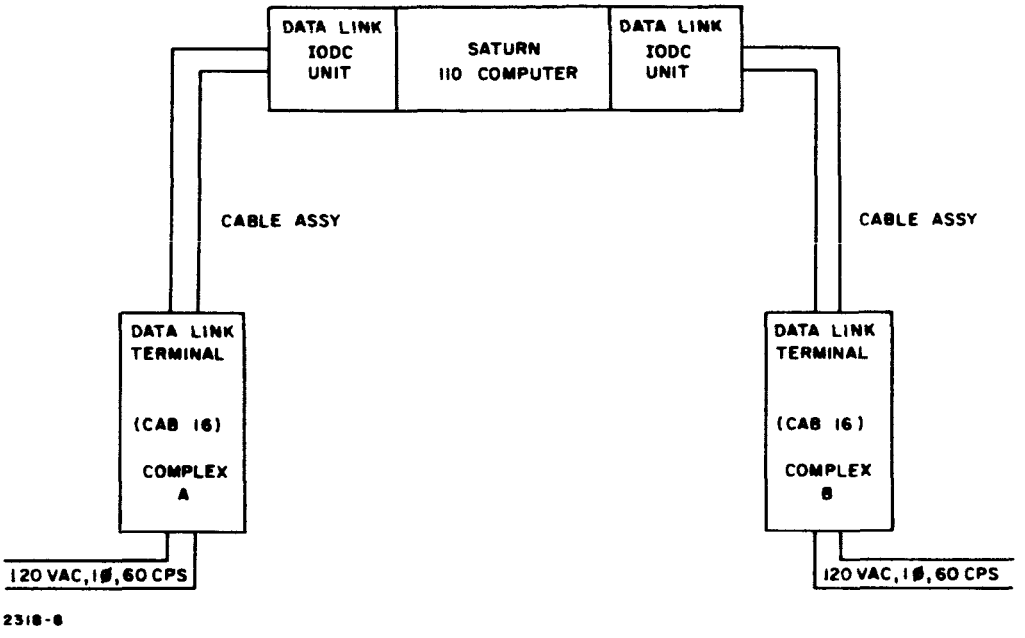


Figure 7-1. Equipment Connection Schematic, Special Test Mode Test or, Acceptance Test

7.2 DATA LINK ACCEPTANCE TEST

The Data Link Acceptance Test provides the user with a reliable test of the RCA 110A Computer Data Link communication system. Figure 7-1 shows the required equipment connection for this test.

The Data Link Acceptance Test is broken into the following subdivisions:

IODC initialization, command channel test without priority interrupt, Duplex check, WDC initialization, RDC initialization, block transfer with priority interrupt, inactivity interrupt, E.O.M. termination, RDC Negative response command test, command channel INOP test and CRL INOP Test. Each subdivision tests the communication link from Complex A to Complex B and from Complex B to Complex A.

Details concerning the acceptance test, and a program listing are contained in NSI 532-1.

7.3 DATA LINK TWO COMPUTER TEST

The purpose of this test is to demonstrate that the Data Link system transfers data between two computers in a simulated tactical situation.

The two computer system uses two independent computer programs, the two programs are loaded into two separate memory locations. The "master" program initiates all test programs and monitors test results. The "slave" program responds to command words received through the cable link between Data Link terminals.

When one computer is used to simulate two computers, IODC 4 represents the Master Program Data Channel and IODC 7 represents the Slave Program Data Channel

When two computers are used, the sense switch selection and loading procedures enable the master program in one and the slave program in the other. Both use their own respective IODC 4.

The equipment connections when one computer is used are shown in Figure 7-2, and for two computers in Figure 7-3. A more detailed program description and a program listing are contained in NSI 532-1.

7.4 RECOMMENDED PROGRAMMING TECHNIQUES

During the generation of programs for this contract, several pitfalls for programs using the Data Link terminals were discovered. If the following recommended techniques are followed the major portion of program errors will be avoided.

1. The status register loaded interrupt request must be serviced and the status register read within 59 milliseconds of the interrupt request or the receiving IODC will go inoperative.

2. An IODC attempting to initiate a block transfer will go inoperative if a response from the remote computer is not received within 59 milliseconds of local IODC initialization.

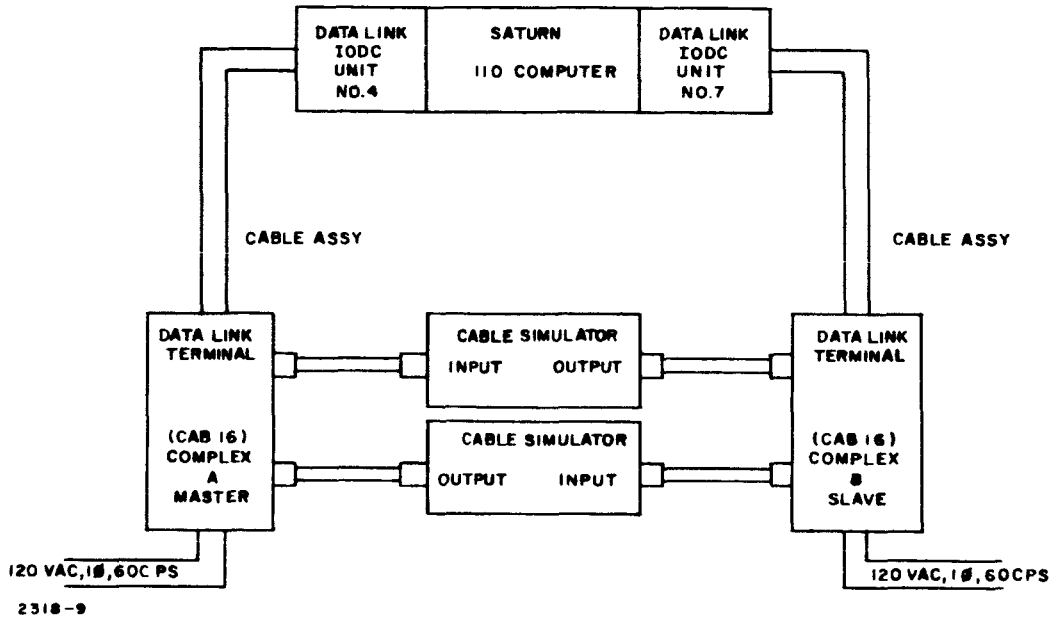


Figure 7-2. Equipment Connection Schematic, Two Computer Simulation

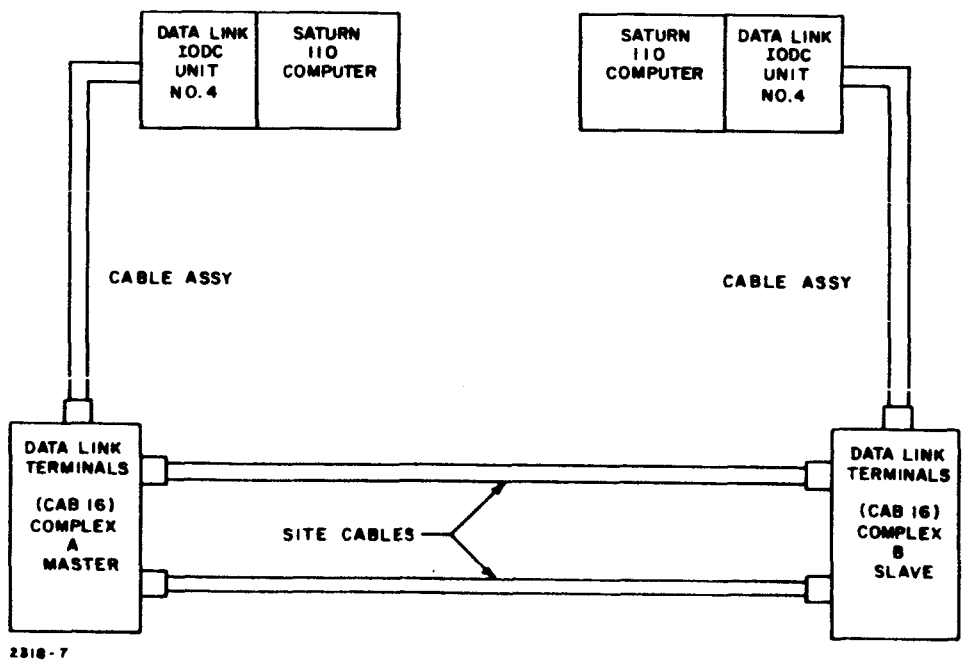


Figure 7-3. Equipment Connection Schematic, Two Computer Configuration

3. A negative response command should be given only in response to the remote computers request.

4. The emergency end of message command should be given only when the local IODC is in the write mode.

5. The status register should be read only if the register is loaded with a command word whose bit 23 is one. The loaded condition is detected by the presence of SRL interrupt or sensing of SRL bit. However, for the later method, it is recommended to sense SRL twice in succession. If both sensings are true, then the status word is loaded with the command word.

6. If bit 23 of the status word is zero, there is an IODC malfunction.

7. The clear status register command should be given only if the register is loaded.

8. The IODC word counter should not be sensed during a data transfer. If the counter must be sensed, it should be sensed twice in succession. If the two readings are not consistant, a third sense should be made.

9. The remote computer's interrupt recognition and service time should be less than 36 RCA 110 computer word times, or the command word transmissions should be separated by 6.3 millisecond plus the interrupt recognition and service time. Otherwise an out of sync condition may occur.

10. The maximum time for a command word to pass from the local to the remote computer is 6.3 milliseconds.

11. If the transmitting terminal goes out of sync within 6.3 milliseconds of a command word transfer, there is a possibility that the command word has been lost.

12. A sequence count should be a part of each command word to permit ready identification of repeated words.

13. The IODC hardware generated command words are also subject to restrictions 9 and 10. These command words are, WDC initiate command word, RDC response command word, and WDC end-of-message command word.

14. The clear command register command should be given only if the register is unloaded or inoperable.

SECTION 8

RECOMMENDATIONS FOR FIELD EVALUATION AND USAGE

All performance evaluations conducted during the Data Link program were performed under laboratory conditions with the aid of a single Saturn 110 Computer. It is recommended that an evaluation program be initiated for the purpose of establishing performance characteristics and verifying the integrity of the Data Link system under actual field operating conditions.

The following paragraphs present some recommendations that would aid such a program.

8.1 WORD ERROR RATE

It is recommended that the average word error rate be defined as the independent variable for tests conducted to establish performance characteristics. This technique is one of convenience and will avoid the requirement of having to define the noise environment. The implication is that actual noise may then be defined in terms of equivalent White Gaussian signal-to-noise ratios. Methods for measuring average word error rates may be found in NSI-532-1.

8.2 NOISE INJECTION

It is recommended that noise injection be employed in the event that actual noise levels are too low to generate word errors. Major portions of the Data Link hardware are not exercised unless errors are generated. This means that portions of the hardware may be inoperable without being detected.

As disclosed in this report the characteristics of the system are greatly dependent on noise generated errors. When testing computer programs, noise should be injected to assure that these characteristics are taken into account.

Procedures for injecting noise may be found in NSI-532-1.

8.3 REDUCED DIPHASE OUTPUT SIGNALS

A figure of merit may be established for the Data Link communication system by operating at reduced Data Modem diphase signal outputs. The Data Modem T-052 Line Amplifier is equipped with an output voltage control, R-10. In normal operation, the output amplitude should be adjusted for maximum output. By reducing the output signal amplitude until some predetermined performance level is achieved, such as 200 word errors per second or a continuous terminal not available signal, the reduction in output signal will constitute an operating "safety margin." Evaluation of this safety margin over a prolonged period of time may disclose long term performance trends.

APPENDIX

DATA LINK CONTROL LOGIC
CALCULATED PERFORMANCE CHARACTERISTICS

This appendix contains a series of mathematical relationships which describe the performance characteristics of the Data Link Control Logic.

Certain assumptions have been made to simplify the calculations. They are:

1. Noise injection on the video cable generates perfectly random bit errors.
2. For system performance which employs two Data Link terminals, the bit errors generated on each of the two video transmission lines are equal and independent.
3. For the bit error rates considered, the probability of a conversion of a repeat request, 01100, to a no repeat request, 10011, is negligible.
4. There are no Retransmission Register parity errors. This assumption is based on the fact that Retransmission Register parity errors would be caused by an equipment malfunction.
5. There are no parity errors for information transfer between the Data Link terminal and the IODC.
6. The IODC is always available to accept data when data is to be transferred to it from the Data Link terminal. In actual operation, if the IODC is not available, the receiving terminal generates a repeat request and system resynchronization may result.

7. It is assumed that the actual time required in the synchronization process is negligable. Actually, at low bit error rates the time required is less than ten word times. At high bit error rates the time is longer because bit errors will interfere with the synchronization process.

Following are definitions of Control Logic performance parameters. These parameters are presented graphically in figures 5-6 through 5-11.

- Pb

  Pb is average bit errors in bit-per-bit.

- Pw

  Pw is the average word errors in word-per-word. This is the probability of a fourty bit word (ARQ character not checked for parity) having an error for a given bit error rate Pb.

- λ bit

  λ bit is the average bit errors in bits-per-second.

  $$\lambda \text{ bit} = \frac{Pb}{4 \times 10^{-6}}$$

- λword

  λword is the average word errors in word-per-second.

  $$\lambda \text{word} = \frac{Pw}{180 \times 10^{-6}}$$

- Pe

  Pe is the average undetected word error rate in word-per-word. This parameter is based on the two dimensional parity error detection scheme employed by the Control Logic.

  $$Pe \quad 280\ Pb^4\ (1 - Pb)^{36}$$

- tbe

  tbe is the average time between undetected word errors in hours

  $$\text{tbe} \quad \frac{1}{Pe \times 5.55 \times 10^3 \times 3.6 \times 10^3}$$

- t

t is the average word information transfer rate in microseconds for a given Pb.

$$t = \left(\sum_{n=0}^{n=\infty} (2n+1)\, P_{(n)} + \sum_{n=0}^{n=\infty} (2n)\, P'_{(n)} \right) \text{ X 180 microseconds.}$$

where:

P(n) is the probability of a word being transmitted n times before being accepted.

$$P(n) = \sum \left(q_0^a \; q_1^b \; P_0^c \; P_1^d \right)$$

where:

$\left(q_0^a \; q_1^b \; P_0^c \; P_1^d \right)$ is a factor computed for a given specific word error transmission sequence. The summation is taken over all the word error sequence combination that can occur for a given word transmission delay factor (2n + 1).

- q0

q0 is the probability of five consecutive ARQ character bits being transmitted and received without error for a given Pb.

$q0 = (1 - Pb)^5$.

- q1

q1 is the probability of the ARQ character being erroneous for a given Pb.

$q1 = 1 - q0$

- P0

P0 is the probability that fourty consecutive bits will be correct for a given Pb.

$P0 = (1 - Pb)^{40}$

- P1

  P1 is the probability that the 40-bit word (ARQ not included) will be in error.

  $P1 = 1 - P0$

- "a"

  "a" is the number of no repeat request ARQ characters received in the given word error transmission sequence.

- "b"

  "b" is the number of repeat request ARQ characters received in the given word error transmission sequence.

- "c"

  "c" is the number of words without error in the given word error transmission sequence.

- "d"

  "d" is the number of words with error in the given word error transmission sequence.

- P'(n)

  P'(n) is the probability of a word being transmitted n times and being ignored.

  $$P'(n) = (q_0^a \; q_1^b \; P_0^c \; P_1^d)$$

  where all parameters are as defined for P(n)

- (2n + 1)

  (2n + 1) is the word transmission time delay factor for the given word error transmission sequence. For example, if a word is accepted on the third transmission the delay factor is five because two of the transmissions were two word retransmissions.

  (2n) is the word transmission time delay factor for the given word error transmission sequence for ignored words.

- T sync

  T sync is the average terminal available time which is the time between Reframing Cycles for the condition where only one of the two terminals in the system are influenced by noise

  $$T \text{ sync} = \frac{180}{P \text{ sync}} \text{ microseconds}$$

  where:

  P sync is the probability of a word being lost because of synchronization.

  $$P \text{ sync} = \sum (q_0^a \; q_1^b \; P_0^c \; P_1^d)$$

  where:

  All parameters are defined as in P(n) except the summation is taken over all word error sequences that result in synchronization.

- T sync normalized

  T sync (normalized) is the average terminal available time in word transmission times.

  $$T \text{ sync (normalized)} = \frac{T \text{ sync in microseconds}}{180 \text{ microseconds}}$$

- T sync (two terminal)

  T sync (two terminal) is average terminal available time for the condition where both terminals in the system are influenced by noise.

  $$T \text{ sync (two terminal)} = \frac{180}{2 \; P \text{ sync}} \text{ microseconds.}$$

- T sync (two terminal) normalized

  T sync (two terminal) normalized is the average terminal available time for two terminals in word transmission times.

  $$T \text{ sync (two terminal) normalized} \quad \frac{T \text{ sync (two terminal) microseconds.}}{180 \text{ microseconds}}$$

- λ sync

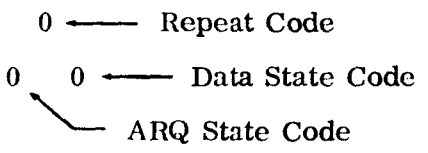
  λsync is the average synchronization rate in synchronizations per second.

$$\lambda sync = \frac{1}{T\ sync\ (two\ terminal)}$$

The values of "t" and "T sync" are based on word error sequences. The following word sequence table, Table 1, is used to systematically derive these sequences.

An explanation is required for the State Code listed for each word sequence in each time slot. The State Code applies to the word directly below it referenced "A", "B" or "C".

The State Code is:



where the Repeat Code is defined as:

0 Original word

1 First word of first retransmission

1' Second word of first retransmission

2 First word of second retransmission

2' Second word of second retransmission

3 First word of third retransmission

3' Second word of third retransmission

Where the Data State Code is defined as:

X Detected noise modification of data has no effect on system response. An example would be that of the second word in a retransmission being

TABLE 1. WORD SEQUENCE TABLE

WORD TRANSMISSION SEQUENCE t																	WORD XMIT TIME DELAYED	NO. OF OCCUR ARQ a	NO. OF OCCUR ARQ b	NO. OF OCCUR DATA c	NO. OF OCCUR DATA d	REMARKS	COMB NO.
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16								
STATE CODE																	1	1	0	1	0	Error Counter (RE) = Repeat Code (RA) RE = RA = 0	1
WORD A																							
STATE CODE	0 1	1 X	1 X 1														3	2	0	1	1	RE = RA at t_3	2
WORD A	B	A																					
STATE CODE	0 1	1 X	1 X 1	1' XX	2 X 0												5	2	0	1	2	RE = RA = 2 at t_5	3
WORD A	B	A	B	A																			
STATE CODE	0 1	1 X	1 X 1	1' XX	2 X 1	2' XX	3 X 0	3' XX	0 0 X								7	3	0	1	3	RE = RA = 3 at t_7	4
WORD A	B	A	B	A	B	A	B	C															
STATE CODE	0 1	1 X	1 X 1	1' XX	2 X 1	2' XX	3 X 0	3' XX	0 1 X								SYNC	2	1	1	3	RE is reset at t_7, RA is incremented at t_9, therefore RA>RE, fourth repeat is requested - sync	5
WORD A	B	A	B	A	B	A	B	C															
STATE CODE	0 1	0 X	1 X 1	1' XX	2 X 1	2' XX	3 X 1										SYNC	2	0	0	4	Remote receiver receives erroneous data for the fourth time - sync	6
WORD A	B	A	B	A	B	A																	
STATE CODE	0 1	1 0	1' X 1														3	1	1	2	1	RE = RA = 0 at t_3	7
WORD B	A	B																					
STATE CODE	0 1	1 1	1 X 1	0 0 X	1 X 0												5	2	1	2	2	RE = RA = 1 at t_5	8
WORD B	A	B	C	B																			
STATE CODE	0 1	1 0	1' X 1	0 0 X	1 X 1	1' XX	2 X 0										7	2	1	2	3	RE = RA = 2 at t_7	9
WORD B	A	B	C	B	C	B																	

TABLE 1. WORD SEQUENCE TABLE (Cont)

	WORD TRANSMISSION SEQUENCE t																WORD XMIT TIME DELAYED	NO. OF OCCUR ARQ a	NO. OF OCCUR ARQ b	NO. OF OCCUR DATA c	NO. OF OCCUR DATA d	REMARKS	COMB NO.
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							
STATE CODE	0 01	1 10	1′ X1	0 0X	1 X1	1′ XX	2 X1	2′ XX	3 X0	3′ XX	0 0X						9	3	1	2	4	RE = RA = 3 at t_8	10
WORD	B	A	B	C	B	C	B	C	B	C	D												
STATE CODE	0 01	1 10	1′ X1	0 0X	1 X1	1′ XX	2 X1	2′ XX	3 X0	3′ XX	0 1X						SYNC	2	2	2	4	RE is reset at t_9, RA is incremented at t_{11} . . . fourth repeat is requested - sync	11
WORD	B	A	B	C	B	C	B	C	B	C	D												
STATE CODE	0 01	1 10	1′ X1	0 0X	1 X1	1 XX	2 X1	2′ XX	3 X1								SYNC	2	1	1	5	Remote receiver receives erroneous data for the fourth time. RE is incremented for the fourth time - sync	12
WORD	B	A	B	C	B	C	B	C	B														
STATE CODE	0 01	1 10	1′ X1	2 1X													SYNC	1	2	1	2	RE is reset at t_2 but RA is incremented at t_4 RA > RE - sync	13
WORD	B	A	B	A																			
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X0												5	2	1	2	2	RE reset at t_4 RE = RA = 0 at t_5	14
WORD	B	A	B	A	B																		
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X1	0 0X	1 X0										7	2	1	2	3	RE reset at t_4 RE = RA = 1 at t_7	15
WORD	B	A	B	A	B	C	B																
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X1	0 0X	1 X1	1′ XX	2 X0								9	2	1	2	4	RE = RA = 2 at t_9	16
WORD	B	A	B	A	B	C	B	C	B														
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X1	0 1X											SYNC	1	2	2	4	RE is reset at t_4, RA is incremented at t_6 . . . RA > RE - sync	17
WORD	B	A	B	A	B	C																	
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X1	0 0X	1 X1	1′ XX	2 X1	2′ XX	3 X0	3′ XX	0 0X				11	3	1	2	5	RE = RA = 3 at t_{11}	18
WORD	B	A	B	A	B	C	B	C	B	C	B	C	D										
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X1	0 0X	1 X1	1′ XX	2 X1	2′ XX	3 X0	3′ XX	0 1X				SYNC	2	2	2	5	RE is reset at t_{11}, RA is incremented at t_{13} . . . RA > RE - sync	19
WORD	B	A	B	A	B	C	B	C	B	C	B	C	D										
STATE CODE	0 01	1 11	1′ XX	2 X0	2′ X1	0 0X	1 X1	1′ XX	2 X1	2′ XX	3 X1						SYNC	2	1	2	6	Remote Receiver receives erroneous data for fourth time - sync	20
WORD	B	A	B	A	B	C	B	C	B	C	B												

TABLE 1. WORD SEQUENCE TABLE (Cont)

WORD TRANSMISSION SEQUENCE																	WORD XMIT TIME DELAYED	NO. OF OCCUR ARQ a	NO. OF OCCUR ARQ b	NO. OF OCCUR DATA c	NO. OF OCCUR DATA d	REMARKS	COMB NO.
	t 1	t 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							
STATE	0	1	1	2	2′	3	3′										7	1	2	3	2	RE reset at t_6 RE = RA = 0 at t_7	21
CODE	01	11	XX	X0	X0	10	XX																
WORD	B	A	B	A	B	A	B																
STATE	0	1	1′	2	2′	3	3′										SYNC	1	2	2	3	RE reset at t_4 RA incremented at t_6 RA > RE - sync	22
CODE	01	11	XX	X0	X0	11	XX																
WORD	B	A	B	A	B	A	B																
STATE	0	1	1′	2	2′	3	3′	0									7	2	1	2	3	RE reset at t_6 RE = RA = 0 at t_7	23
CODE	01	11	XX	X1	XX	X0	X0	0X															
WORD	B	A	B	A	B	A	B	C															
STATE	0	1	1′	2	2′	3	3′	0									SYNC	1	2	2	3	RE reset at t_6, RA incremented at t_8 ∴ RA > RE - sync	24
CODE	01	11	XX	X1	XX	X0	X0	1X															
WORD	B	A	B	A	B	A	B	C															
STATE	0	1	1′	2	2′	3	3′										SYNC	1	1	1	4	Remote receiver receives erroneous data for fourth time - sync	25
CODE	01	11	XX	X1	XX	X0	X1																
WORD	B	A	B	A	B	A	B																
STATE	0	1	1′	2	2′	3											SYNC	1	1	0	4	Remote receiver receives erroneous data for fourth time - sync	26
CODE	01	11	XX	X1	X0	X1																	
WORD	B	A	B	A	B	A																	
STATE	1																2	0	1	1	0	RE = 0 RA = 1 Two words are ignored	27
CODE	10																						
WORD	B																						
STATE	1	1	2														4	0	1	1	1	RE = 1 RA = 2 Four words are ignored	28
CODE	11	XX	X0																				
WORD	B	C	B																				
STATE	1	1′	2	2′	3	3′	0										6	1	1	1	2	RE = 2 RA = 3 Six words are ignored	29
CODE	11	XX	X1	XX	X0	XX	0X																
WORD	B	C	B	C	B	C	D																
STATE	1	1′	2	2′	3	3′	0										SYNC	0	2	1	2	RE reset at t_5 RA incremented at t_7 ∴ RA > RE - sync	30
CODE	11	XX	X1	XX	X0	XX	1X																
WORD	B	C	B	C	B	C	D																
STATE	1	1′	2	2′	3	3′											SYNC	0	1	0	3	Remote receiver receives third data retransmission containing error-sync	31
CODE	11	XX	X1	XX	X1	XX																	
WORD	B	C	B	C	B	C																	

erroneous and the first word in the retransmission being rejected because of error. This is a "don't care" condition.

1 Detected noise modification of data has an effect on system response.

0 There is no noise modification of the data.

Where the ARQ State Code is:

X Noise modification of an ARQ character has no effect on system response. Under our assumptions, an example would be the transmission and reception of a repeat request. The noise would not convert this character to a no repeat request. Another example would be the ARQ character for the second word of a retransmission.

1 Noise modification of an ARQ character has an effect on system response. The condition is the transmission of a no repeat request which is modified by noise and received as a repeat request ARQ.

0 No noise modification of the ARQ is experienced. The condition would be the transmission and reception of a no repeat request ARQ.

As an example of how to interpret the word transmission sequence state code, consider the first five word transmission times listed for combination 4. The sequence is:

t1	t2	t3	t4	t5
0	0	1	1'	2
0 1	0 X	X 1	X X	X 1
A	B	A	B	A

At t1 original word A is received at remote terminal because during previous time slot the local terminal did not receive a repeat request. The original word A is found to have an error.

At t2, original word B is received at remote terminal because during t1 the local terminal did not receive a repeat request. The word is ignored by the remote terminal because the previous word A was erroneous.

At t3, repeated word A is received at remote terminal because during t2 the local terminal received a repeat request for word A which was received and found to be in error during t1. The repeated word A is found to have an error.

At t4, repeated word B is received at remote terminal because it follows repeated word A. The ARQ received at the local terminal was ignored since, if a word is retransmitted, the following word is automatically retransmitted. The repeated word B is ignored by the remote terminal because A received at t3 was erroneous.

At t5, word A is received for the third time at the remote terminal because during t4 the local terminal received a repeat request for word A. The repeated word A is found to be in error for the third time.

The definition of "a" is the number of no repeat request ARQ characters received in the given transmission sequence. The "b" is the number of repeat request ARQ characters received. "c" is the number of words without error. "d" is the number of words with error.

The following computation table, Table 2, is used to assist in computing the values of "t" and T sync for a given Pb. The table must be completed for each value selected for Pb.

TABLE 2.
COMPUTATION TABLE

Pb =

P(n) AND P'(n)	TIME DELAY FACTOR	COMB NO.	a	b	c	d	q_0^a	q_1^b	P_0^c	P_1^d	$q_0^a q_1^b P_0^c P_1^d$
P(0)	1	1	1	0	1	0	q_0	1	P_0	1	P(0) = Sub Total
P(1)	3	2	2	0	1	1	q_0^2	1	P_0	P_1	
		7	1	1	2	1	q_0	q_1	P_0^2	P_1	P(1) = Sub Total
P(2)	5	3	2	0	1	2	q_0^2	1	P_0	P_1^2	
		8	2	1	2	2	q_0^2	q_1	P_0^2	P_1^2	
		14	2	1	2	2	q_0^2	q_1	P_0^2	P_1^2	P(2) = Sub Total
P(3)	7	4	3	0	1	3	q_0^3	1	P_0	P_1^3	
		9	2	1	2	3	q_0^2	q_1	P_0^2	P_1^3	
		15	2	1	2	3	q_0^2	q_1	P_0^2	P_1^3	
		21	1	2	3	2	q_0	q_1^2	P_0^3	P_1^2	
		23	2	1	2	3	q_0^2	q_1	P_0^2	P_1^3	P(3) = Sub Total

TABLE 2.
COMPUTATION TABLE (Cont)

Pb =

P(n) AND P'(n)	TIME DELAY FACTOR	COMB NO.	a	b	c	d	q_0^a	q_1^b	P_0^c	P_1^d	$q_0^a q_1^b P_0^c P_1^d$
P(4)	9	10	3	1	2	4	q_0^3	q_1	P_0^2	P_1^4	
		16	2	1	2	4	q_0^2	q_1	P_0^2	P_1^4	P(4) = Sub Total
P(5)	11	18	3	1	2	5	q_0^3	q_1	P_0^2	P_1^5	P(5) = Sub Total
P'(1)	2	27	0	1	1	0	1	q_1	P_0	1	P'(1) = Sub Total
P'(2)	4	28	0	1	1	1	1	q_1	P_0	P_1	P'(2) = Sub Total
P'(3)	6	29	1	1	1	2	q_0	q_1	P_0	P_1^2	P'(3) = Sub Total

TABLE 2.
COMPUTATION TABLE (Cont)

Pb =

P SYNC	TIME DELAY FACTOR	COMB NO.	a	b	c	d	q_0^a	q_1^b	P_0^c	P_1^d	$q_0^a\ q_1^b\ P_0^c\ P_1^d$
	Sync	5	2	1	1	3	q_0^2	q_1	P_0	P_1^3	
	Sync	6	2	0	0	4	q_0^2	1	1	P_1^4	
	Sync	11	2	2	2	4	q_0^2	q_1^2	P_0^2	P_1^4	
	Sync	12	2	1	1	5	q_0^2	q_1	P_0	P_1^5	
	Sync	13	1	2	1	2	q_0	q_1^2	P_0	P_1^2	
	Sync	17	1	2	2	4	q_0	q_1^2	P_0^2	P_1^4	
	Sync	19	2	2	2	5	q_0^2	q_1^2	P_0^2	P_1^5	
	Sync	20	2	1	2	6	q_0^2	q_1	P_0^2	P_1^6	
	Sync	22	1	2	2	3	q_0	q_1^2	P_0^2	P_1^3	
	Sync	24	1	2	2	3	q_0	q_1^2	P_0^2	P_1^3	
	Sync	25	1	1	1	4	q_0	q_1	P_0	P_1^4	
	Sync	26	1	1	0	4	q_o	q_1	1	P_1^4	
	Sync	30	0	2	1	2	1	q_1^2	P_0	P_1^2	
	Sync	31	0	1	0	3	1	q_1	1	P_1^3	P sync = Total